Who we are

- We are the semiconductor device modeling group which is part of MSCAD laboratory at University of Arkansas, Fayetteville.
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1. Overview of UARK SiC Power MOSFET model

2. The SiC Power MOSFET model presented here is based on the analytical model published in [1] and [2]. A 1200 V, CREE device (C2M0025120D) has been used in this work to illustrate the parameter extraction and model validation. Chapter 2 explains the process of parameter extraction sequence using the device datasheet and Chapter 3 shows the model validation using double pulse tester circuit. Chapter 4 shows the comparison between MAST and Verilog-A codes of the model. Chapter 5 entails all the parameters used in the model and Chapter 6 comprises of the model equations. Finally, chapter 7 includes the people involved in this project.

References:


Sponsor:

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2. Parameter Extraction Sequence

The SiC Power MOSFET model parameters are extracted in a set sequence such that only the characteristics that are readily available in the device datasheets of most commercial devices are required. In the absence of device datasheets, the user may be required to measure the device characteristics to extract the device model parameters.

The parameter extraction sequence requires the following device characteristics in the given order for the extraction of useful parameters for any transient simulation or power electronic application.

1) Capacitance vs. Voltage Characteristics (also referred to as CV characteristics)
2) Device Transfer Characteristics (also referred to as \( I_d - V_{gs} \) Characteristics)
3) Device Output Characteristics (also referred to as \( I_s - V_{ds} \) Characteristics)

To demonstrate the parameter extraction sequence, the characteristics from a commercially available datasheet of the 1200 V CREE power MOSFET (C2M0025120D) are used.

1) Capacitance vs. Voltage Characteristics:

The parameters which must be adjusted to fit the CV characteristics are listed in the order below:

- \( C_{RSS} \) Curve: \( C_{oxd} \), \( V_{td} \), \( n_b \), and \( a_{gd} \)
- \( C_{OSS} \) Curve: \( C_{ds} \), and \( m \)
- \( C_{ISS} \) Curve: \( C_{gs} \)

Fig. 1(a) shows the test schematic used to simulate the CV characteristics and Fig. 1(b) shows the CV characteristics for the C2M0025120D CREE device and the simulated characteristics after the extraction of the aforementioned parameters. The plots also reveal the regions within the curves that are affected by the parameters as shown in [2].
Fig. 1 (a) Test circuit implemented in Saber® simulator for C-V characteristics
2) Device Transfer Characteristics

The parameters which must be adjusted to fit the \( I_d-V_{gs} \) characteristics are listed below: \( r_s, k_{ph}, k_{pl}, \) and \( v_t \).

Fig. 2(a) shows the test schematic used to simulate the Device Transfer Characteristics and Fig. 2(b) shows the transfer characteristics for the C2M0025120D CREE device and the simulated characteristics after the extraction of the aforementioned parameters. The extraction of the parameters is performed by adjusting the parameters in the appropriate regions of the curve as indicated in the figure [1] and [2].
Fig. 2 (a) Test circuit implemented in Saber® simulator for dc characteristics
3) Device Output Characteristics:
   The parameters which must be adjusted to fit the output characteristics are listed below:
   \( k_fh \), \( k_n \), and \( p_{vf} \)

   Fig. 3 shows the output characteristics for the C2M0025120D CREE device and the simulated characteristics after the extraction of the aforementioned parameters. Fig. 3 also shows the regions within the output characteristics which are directly affected by the adjustment of the listed parameters as shown in [2].
The described parameter extraction strategy is performed at room temperature, using $T = T_{\text{Nom}}$ in the model. To extract the temperature scaling parameters, the same extraction is performed at several temperature increments and the model temperature $T$ is set equal to the simulation temperature in each case. Only the parameters which have temperature scaling are extracted at each temperature, and the rest of the parameters are fixed to their room temperature values. Finally, values for the temperature scaled parameters are obtained at several temperature points. Then, using the temperature scaling equations of the model, the temperature scaling parameters ($k_{p\text{htexp}}, k_{p\text{ltesp}}, k_{f\text{htexp}}, k_{f\text{ltexp}}, \theta_{\text{htexp}}, \theta_{\text{ltesp}}, v_{\text{htco}}, v_{\text{ltesp}}$) are extracted using the parameter values as function of the temperature.
Fig. 4 Simulated and datasheet transfer characteristics for C2M0025120D CREE device at 150°C
Fig. 5 Simulated and datasheet output characteristics for C2M0025120D CREE device at 150°C
3. Transient Simulation:

Fig. 6 (a) Double pulse test schematic in Saber®
After the extraction of useful parameters, the model is validated for transient simulations using a double-pulse tester switching circuit as shown in Fig. 6 (a). The dynamic current and voltage characteristics using a clamped inductive load are shown in fig. 6(b) and 6 (c), respectively.

![Transient Drain Current](chart.png)

**Fig. 6(b)** Simulated and measured transient drain current using double pulse tester
Fig. 6 (c) Simulated and measured transient drain-source voltage using double pulse tester
4. Comparison between Verilog-A and MAST codes

Comparison between Verilog-A and MAST code simulation for $I_d$-$V_{ds}$:

Figure 7(a): $I_d$-$V_{ds}$ characteristics comparison between Verilog-A and MAST codes
Comparison between Verilog-A and MAST code simulation for $I_d-V_{gs}$:

Figure 7(b): $I_d$-$V_{gs}$ characteristics comparison between Verilog-A and MAST codes
Comparison between Verilog-A and MAST code simulation for Input Capacitance ($C_{iss}$):

![Graph showing comparison between Verilog-A and MAST for Input Capacitance ($C_{iss}$)]

Figure 7(c): Input Capacitance ($C_{iss}$) characteristics comparison between Verilog-A and MAST
Comparison between Verilog-A and MAST code simulation for Input Capacitance ($C_{iss}$):

![Graph showing comparison between Coss_MAST_vs_verilogA](image)

Figure 7(d): Output Capacitance ($C_{oss}$) characteristics comparison between Verilog-A and MAST
Comparison between Verilog-A and MAST code simulation for Reverse Transfer Capacitance ($C_{rs}$):

![Graph showing Comparison between Verilog-A and MAST code simulation for Reverse Transfer Capacitance ($C_{rs}$).](image)

**Figure 7(e):** Reverse Transfer Capacitance ($C_{rs}$) characteristics comparison between Verilog-A and MAST
Transient characteristics comparison Verilog-A and MAST codes using double pulse test in Spectre:

Figure 7(f): Comparison of transient $V_{ds}$ characteristics between MAST in Saber and Verilog-A in Spectre simulations
Figure 7(g): Comparison of transient $I_d$ characteristics between MAST in Saber and Verilog-A in Spectre simulations
5. **Synchronous mode:**

When synchronous mode is activated the model supports both first and third quadrant of MOSFET characteristics. This mode incorporates internal bodydiode of PowerFET.

![Synchronous mode DC-characteristics](image)

*Figure 8: Synchronous mode DC-characteristics for C2M0025120D CREE device at 25°C*
6. **Parameter list:**

The parameters that were used to build up the PowerFET model are listed below:

<table>
<thead>
<tr>
<th>Parameter name</th>
<th>Default value</th>
<th>Unit</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mtrlmod</td>
<td>1</td>
<td></td>
<td>Material type: &quot;0&quot; corresponds to Si and &quot;1&quot; corresponds to SiC</td>
</tr>
<tr>
<td>Syncmod</td>
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<td>Mode type: &quot;0&quot; corresponds to synchronous operation disabled and &quot;1&quot; corresponds to synchronous operation enabled.</td>
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<tr>
<td>cgs</td>
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<td>F</td>
<td>Gate to source capacitance</td>
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<tr>
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<td>F</td>
<td>Drain to source zero bias capacitance</td>
</tr>
<tr>
<td>cgdo</td>
<td>1e-12</td>
<td>F</td>
<td>Gate drain overlap capacitance</td>
</tr>
<tr>
<td>coxd</td>
<td>7e-9</td>
<td>F</td>
<td>Gate oxide capacitance</td>
</tr>
<tr>
<td>vtd</td>
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<td>V</td>
<td>Gate drain overlap depletion threshold voltage</td>
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<td>V/K</td>
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</tr>
<tr>
<td>fc</td>
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<td></td>
<td>Forward-bias depletion capacitance coefficient</td>
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<tr>
<td>m</td>
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<td></td>
<td>Junction grading coefficient</td>
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<td>cm$^2$</td>
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<td>Empirical parameter to model transconductance reduction low gate-source voltage</td>
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<td></td>
<td>Empirical parameter to model transconductance reduction for high gate-source voltage</td>
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<td></td>
<td>Value</td>
<td>Description</td>
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<td>--------</td>
<td>--------------------------------------------------</td>
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<td>thetaltempx</td>
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</tr>
<tr>
<td>thetahtempx</td>
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<td>Temperature exponent for thetah</td>
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<tr>
<td>rs</td>
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<td>Parasitic drain resistance</td>
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<tr>
<td>kfl</td>
<td>12</td>
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<td>kfh</td>
<td>5</td>
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<td>kpl</td>
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<td>Temp. exponent for kfh</td>
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<td>Temp. exponent for kpl</td>
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<tr>
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<td>Temp. exponent for kph</td>
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<tr>
<td>vtl</td>
<td>3.7 V</td>
<td>Low current threshold voltage</td>
<td></td>
</tr>
<tr>
<td>vth</td>
<td>32e-3 V</td>
<td>High current threshold voltage</td>
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<tr>
<td>vtltco</td>
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<td>Temp. coefficient of vtl</td>
<td></td>
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<tr>
<td>vthtco</td>
<td>0 V/K</td>
<td>Temp. coefficient of vth</td>
<td></td>
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<td>vbigd</td>
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<td>Gate-drain neck region built-in potential</td>
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<td>pvf</td>
<td>440e-3</td>
<td>Pinch-off voltage parameter to adjust drain-source saturation voltage</td>
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<td>fxjbe</td>
<td>0.5 F/cm²</td>
<td>Fraction depletion charge at gate-drain overlap edge</td>
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</tr>
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<td>fxjbm</td>
<td>0.75 F/cm²</td>
<td>Fraction depletion charge at gate-drain overlap middle</td>
<td></td>
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<tr>
<td>slmin</td>
<td>1e-9 A/V</td>
<td>Minimum slope for MOSFET current</td>
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<tr>
<td>id0</td>
<td>0 A</td>
<td>Leakage current at breakdown voltage</td>
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<tr>
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<td>Breakdown voltage of the device</td>
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<tr>
<td>tnom</td>
<td>27 °C</td>
<td>Nominal temperature</td>
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<tr>
<td>rd</td>
<td>13e-3 Ω</td>
<td>Parasitic drain resistance</td>
<td></td>
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<tr>
<td>rdvd</td>
<td>0 Ω/V</td>
<td>Drain voltage coefficient of drift resistance</td>
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</tr>
<tr>
<td>rdvg11</td>
<td>0 Ω/V</td>
<td>First gate voltage coefficient of drift resistance</td>
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</tr>
<tr>
<td>rdvg12</td>
<td>1.0 Ω/V</td>
<td>Second gate voltage coefficient of drift resistance</td>
<td></td>
</tr>
<tr>
<td>Parameter</td>
<td>Value</td>
<td>Unit</td>
<td>Description</td>
</tr>
<tr>
<td>---------------</td>
<td>-------</td>
<td>------------</td>
<td>--------------------------------------</td>
</tr>
<tr>
<td>rdtemp1</td>
<td>0</td>
<td>Ω/𝐾</td>
<td>First temperature coefficient of rd</td>
</tr>
<tr>
<td>rdtemp2</td>
<td>0</td>
<td>Ω/𝐾</td>
<td>Second temperature coefficient of rd</td>
</tr>
<tr>
<td>rdvdtemp1</td>
<td>0</td>
<td>Ω/𝑉.𝐾</td>
<td>First temperature coefficient of rdvd</td>
</tr>
<tr>
<td>rdvdtemp2</td>
<td>0</td>
<td>Ω/𝑉.𝐾</td>
<td>Second temperature coefficient of rd</td>
</tr>
<tr>
<td>kvsg1</td>
<td>0</td>
<td>1/𝑉</td>
<td>Gate bias dependent first body diode parameter</td>
</tr>
<tr>
<td>kvsg2</td>
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<td>1/𝑉</td>
<td>Gate bias dependent second body diode parameter</td>
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<tr>
<td>nd</td>
<td>1.0</td>
<td></td>
<td>Emission coefficient of body diode</td>
</tr>
</tbody>
</table>
7. Symbolic equivalent circuit of the model:
8. Equations:

The equations that have been used in the model are given below:

**Permittivity, intrinsic carrier concentration and mobility calculation for Si**

\[
\begin{align*}
\epsilon &= \epsilon_0 \times \epsilon_{rsi} \\
n_i &= \frac{3.88 \times 10^{16} \times (\text{temperature})^{1.5}}{\exp\left(\frac{7000}{\text{temperature}}\right)} \\
m_{un} &= \frac{5.1 \times 10^{18} + 92 \times n_b^{0.91}}{(3.75 \times 10^{15} + n_b^{0.91}) \times \left(\frac{300}{\text{temperature}}\right)^{2.5}}
\end{align*}
\]

**Permittivity, intrinsic carrier concentration and mobility calculation for SiC**

\[
\begin{align*}
\epsilon &= \epsilon_0 \times \epsilon_{rsic} \\
n_i &= \frac{1.7 \times 10^{16} \times \text{temperature}^{1.5}}{2.08 \times 10^4 e^{2.08 \times 10^4 / \text{temperature}}} \\
m_{un} &= \frac{947}{\left(1 + \left(\frac{n_b}{1.94 \times 10^{17}}\right)^{0.61}\right) \times \left(\frac{\text{temperature}}{300}\right)^{-2.15}}
\end{align*}
\]

**Voltage definition**

\[\text{Drain to internal drain voltage, } \text{vddnr} = \text{V(res_drain)}\]

\[\text{Internal drain to internal source voltage, } \text{vdnrsnr} = \text{V(imos_intrinsic)}\]
Internal source to source voltage, \(v_{snrs} = V(res\_source)\)

gate to internal source voltage, \(v_{gsnr} = V(cap\_gs)\)

Gate to internal drain voltage, \(v_{gdnr} = V(cap\_gd)\)

Drain to source voltage, \(v_{ds} = v_{ddnr} + v_{dnrsnr} + v_{snrs}\)

Internal drain to gate voltage, \(v_{dnrg} = (-1) \times v_{gdnr}\)

Voltage across bodydiode resistance, \(v_{diodnr} = V(res\_bdiode)\)

Voltage across bodydiode, \(v_{bdiod} = V(cap\_ds)\)

Current calculation through parasitic resistance

\[
ires\_drain = \frac{v_{ddnr}}{r_{drift}}
\]

\[
ires\_source = \frac{v_{snrs}}{r_{s}}
\]

\[
ires\_bdiode = \frac{v_{diodnr}}{res\_bdiode}
\]

Mosfet low current in triode region

\[
imosl = \frac{k_{fl} \times k_{pl} \times \left( \left( v_{gsnr} - v_{tl} \right) \times v_{dnrsnr} - \left( p v_{f} y_{l} - 1 \times v_{dnrsnr} y_{l} \times \frac{v_{gsnr} - v_{tl}}{y_{l}}\right) \right)}{1 + \theta_{tal} \times (v_{gsnr} - v_{tl})}
\]
Mosfet low current in saturation region

\[ imosl = \frac{kpl \times (vgsnr - vtl)^2}{2 \times (1 + thetal \times (vgsnr - vtl))} \]

Mosfet high current in triode region

\[ imosh = \frac{kfh \times kph \times \left( (vgsnr - vth) \times vdnrsnr - \left( pvf^{yh-1} \times vdnrsnr^{yh} \times \frac{(vgsnr - vth)^2 - yh}{yh} \right) \right)}{1 + thetah \times (vgsnr - vth)} \]

Mosfet high current in saturation region:

\[ imosh = \frac{kph \times (vgsnr - vth)^2}{2 \times (1 + thetah \times (vgsnr - vth))} \]

Total Mosfet current:

\[ imos = mode \times ((imosl + imosh) + slmin \times vdnrsnr) \]

In case of synchronous rectification is enabled, mode is negative for third quadrant characteristics.

Bodydiode current:

\[ tmp1 = \text{limexp}(-vbdioode/(nd \times vth)) \]

\[ tmp2 = \text{limexp}(-(kvsg2 \times vgsnr)) \]
\[ i_{b\text{diode}} = i_{s_{\text{body}}} \times \text{tmp2} \times (\text{tmp1} - 1) \]

**Drain to source capacitance calculation**

\[
c_{\text{dsdep}} = \begin{cases} 
  c_{\text{ds}} \times \left( \frac{v_{\text{bi}}}{v_{\text{bi}} + v_{\text{bdiode}}} \right)^m, & \text{if } v_{\text{bdiode}} + v_{\text{bi}} > 0 \\
  c_{\text{ds}}, & \text{elsewhere}
\end{cases}
\]

\[
q_{\text{cds}j} = \begin{cases} 
  c_{\text{ds}} \times v_{\text{bi}}^m \times \frac{(v_{\text{bi}} + v_{\text{bdiode}})^{(1-m)} - v_{\text{bi}}^{(1-m)}}{(1-m)}, & \text{if } v_{\text{bdiode}} + v_{\text{bi}} > 0 \\
  c_{\text{dsdep}} \times v_{\text{bdiode}}, & \text{elsewhere}
\end{cases}
\]

**Two-phase gate to drain capacitance calculation**

\[
w_{\text{gdj}} = \begin{cases} 
  0, & \text{if } v_{\text{dnr}g} + v_{\text{td}} \leq 0 \\
  \sqrt{2 \times \epsilon_{\text{ps}} \times \frac{v_{\text{dnr}g} + v_{\text{td}}}{q \times n_b}}, & \text{elsewhere}
\end{cases}
\]

\[
c_{\text{gd}} = \begin{cases} 
  \epsilon_{\text{ox}}d, & \text{if } v_{\text{dnr}g} + v_{\text{td}} \leq 0 \\
  \epsilon_{\text{ox}}d \times \frac{c_{\text{gdj}}}{\epsilon_{\text{ox}}d + c_{\text{gdj}}}, & \text{elsewhere}
\end{cases}
\]
\[ q_{cdg} = \begin{cases} 
   c_{oxd} \times v_{dnrg}, & \text{if } v_{dnrg} + v_{td} \leq 0 \\
   c_{gd} \times v_{dnrg}, & \text{elsewhere} 
\end{cases} \]

Gate to source charge, \( q_{cgs} = c_{gs} \times v_{gsnr} \)

Datasheet capacitance definitions

\[
\begin{align*}
   c_{iss} &= c_{gd} + c_{gs} \\
   c_{oss} &= c_{gd} + c_{dsdep} \\
   c_{rss} &= c_{gd}
\end{align*}
\]

Temperature scaling equations

\[
\begin{align*}
   t_{diff} &= \text{temperature} - t_{nom} \\
   t_{ratio} &= \frac{\text{temperature}}{t_{nom}} \\
   k(\text{temperature}) &= k(\text{tnom}) \times t_{ratio}^{-k_{\text{exp}}} \\
   \theta(\text{temperature}) &= \theta(\text{tnom}) \times t_{ratio}^{\theta_{\text{exp}}} \\
   v_{t(\text{temperature})} &= v_{t(\text{tnom})} + t_{diff} \times v_{tco}
\end{align*}
\]
9. People Involved

1) Mihir Mudholkar
2) Shamim Ahmed
3) Ty McNutt
4) Ramchandra Kotecha
5) Arman-Ur-Rashid
6) Mr. Tom Vrotsos
7) Prof. Alan Mantooth