Effects of Parylene Coating on Electron Transport in Pristine Suspended Carbon Nanotube Field-Effect-Transistors

Max L. Wang, Jihan Chen, Moh Amer, Stephen Cronin, Adam Bushmaker

***Abstract*— Carbon nanotube field effect transistors are anticipated to provide a viable alternative to silicon as CMOS technology begins to reach ultimate scaling lengths. With high carrier mobilities, current density, and tunable bandgaps, carbon nanotubes can allow for the growth of the transistor industry beyond traditional materials. However, these nanotubes are sensitive to their surroundings and require a protective passivation layer to isolate them from contamination by their external environment. Thin parylene films have been shown to be a practical passivation layer for carbon nanotube devices as a flexible, chemically inert, high dielectric strength, pinhole-free material. In this paper, we perform electrical characterization of single suspended carbon nanotube field effect transistors before and after passivation with parylene-C thin film deposition. Analysis shows moderate changes in the threshold voltage, subthreshold slope, and On/Off ratio with parylene passivation, indicating minimal effect on the carbon nanotube field effect transistor overall performance.**

***Index Terms*— Carbon nanotube (CNT), Transistors, Parylene, Passivation, Statistical analysis, Coatings, Interface phenomena, Flexible electronics**

I. Introduction

Carbon nanotubes (CNTs) have become the subject of increasing research in the past few decades due to their unique fundamental properties. These properties include exceptionally high intrinsic carrier mobilities [1] (~100,000 cm^2/Vs), elastic moduli [2] (~1 TPa), and thermal conductivities [3] (~6,000 W/mK). In addition, with single nanometer diameters, these tubes can act as quasi-1D conductors in which electrons can travel with very low scattering rates and large current carrying capacity [4]. CNTs can be metallic or semiconducting with a tunable band gap, depending on chirality [5]. This tunability along with the exceptional material properties makes CNTs a viable alternative to silicon as a channel material for future field effect transistor technologies, including flexible electronics [6], nonvolatile memory [7], amplifiers [8], and many other novel devices [9-14].

One of the challenges that CNTs face is that they are sensitive to their external environment due to high current density on the surface. As a result, a passivation layer is required to protect the CNTs against external factors such as atmospheric oxygen and water vapor [15]. Many different passivation materials have been tested including polymethyl-methacrylate (PMMA) [16], hafnium oxide [17], silicon nitride [18], self-assembled monolayers such as HMDS [19], and aluminum oxide [20-22]. Following Selvarasah's et al. observations [15], each of these materials has its own drawbacks. With PMMA, hysteresis was observed and correlated to ambient humidity. This is because of the water molecules' ability to permeate through the PMMA. Silicon nitride and aluminum oxide films use catalytic chemical vapor deposition and atomic layer deposition, respectively, which require elevated temperatures, limiting their application in flexible technologies. Finally, many of these manufacturing processes show significant hysteresis before and after passivation. Exceptions include aluminum oxide [21], and HDMS self-assembled monolayers [19].

On the other hand, parylene or poly(para-xylylene) is a chemically inert, high dielectric strength, pinhole-free material. It is hydrophobic and dense enough to protect against moisture and gases as well as corrosive substances. [10, 15] The deposition process occurs at room temperature under medium vacuum (low milliTorr range) creating a uniform conformal coating that is able to encapsulate complex geometries [23]. These characteristics make it invaluable to the automotive, electronics, medical, and aerospace communities, covering everything from sensors and circuit boards to catheters and stents [24]. Parylene passivation has recently been used on CNT transistors in the search for flexible and transparent transistors. Because parylene can be deposited at room temperature it will not damage the underlying substrate (usually plastic for flexible electronics) [25]. Additionally, because of the conformal coating, parylene could potentially be used to form an all-around (low-k) gate dielectric for a coaxial CNT FET. Until now, the main focus of parylene passivated CNT transistors has been to study its resilience to stress and strain [25, 26] for flexible electronics applications. Results have shown thatOn currents decrease slightly during bending but completely recover afterwards

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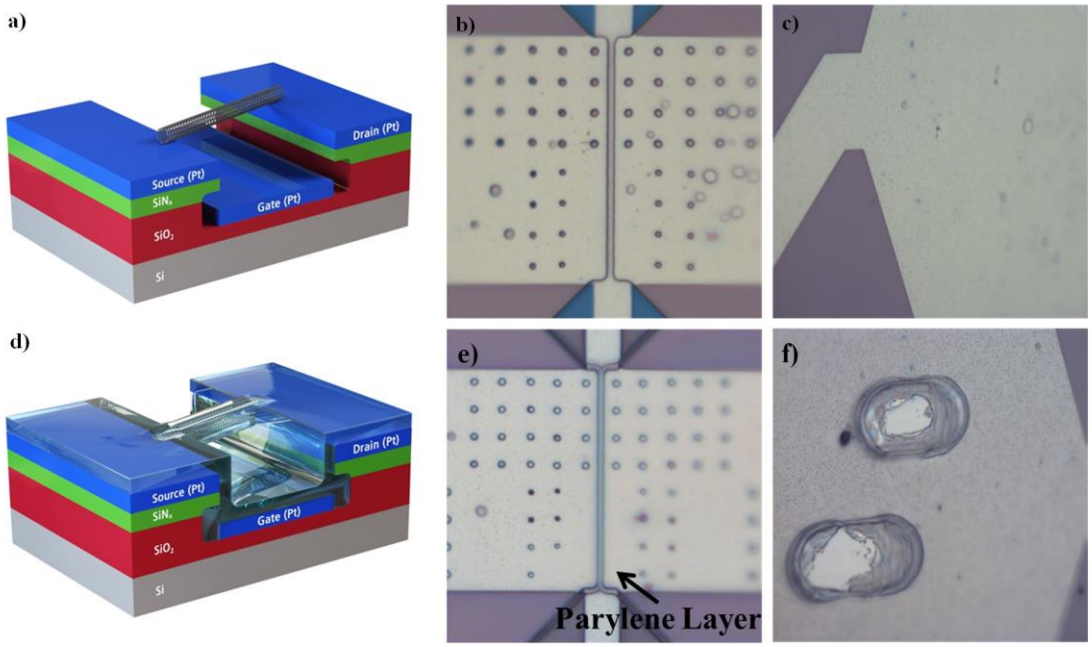

Fig. 1. Device schematic and optical microscope images of CNTFET. a) Device schematic, b) 500 nm channel, and c) contact pads before and d), e), and f) after parylene passivation with pockets made for probing. The parylene layer can clearly be seen in e) and f) and covers the entire device.

[25]. Stress-strain measurements with simultaneous electrical characterization show the CNT resistance increasing to 800% as strain was increased to failure at a strain of 7.5% [26]. The elastic modulus was around 2 GPa, limited by parylene. Selvarasah et al. [15] measured resistance, ON current, and hysteresis width before and after parylene passivation, showing thatOn currents and hysteresis decreased while two terminal resistance increased. Subthreshold swing, Off current, andOn/Off ratio were not investigated. Notably, the CNT transistors in this study also started with a parylene gate oxide, severely limiting the ability to evaluate the fundamental effects of parylene coatings on the CNT channel. Finally, Marty et al. studied CNT FETs coated with parylene and HfO_x [27]. This study focused primarily on assessing the performance of top-gates patterned after dielectric deposition. Consequently, data for evaluating the effects of parylene deposition alone are missing. Thus, there has not been a clear comprehensive comparison of electrical properties of these CNT MOSFETs (CNTFETs) before and after passivation.

Many current applications of CNT technology and research utilize unorganized CNT arrays. Previous research on parylene passivation of CNTFETs by Selvarasah et al. [15], Chen et al. [26, 28], and Artukovic et al. [25] focused on CNT arrays. Though these arrays have many beneficial attributes, their electrical properties are still far inferior to those of individual CNTs [8]. Besides the diminished electrical properties, these arrays are deposited directly onto the substrate below. Non-suspended CNTs can exhibit noise [29] and other undesirable effects [30] caused by CNT-substrate interactions, hiding any effects from subsequent parylene deposition [31]. In addition, CNT arrays obfuscate experimental results by averaging across many CNTs.

Here we study the electrical effects of a parylene passivation layer on CNTFETs using individual, pristine semiconducting suspended single-walled CNT channel devices (Figure 1). These devices have much better properties than unorganized CNT array-based devices, and experiments performed on identical devices in previous research efforts have demonstrated robust observation of sensitive phenomena such as Wigner crystal formation [32], Mott insulation [33], breakdown of the Born Oppenheimer approximation [34], and direct observation of non-equilibrium phonon populations [35, 36]. As such, these devices are ideal candidates on which to study the perturbative effects of parylene passivation on electrical transport behavior. It should be noted, however, that parylene has a relatively low dielectric constant, and thus in a high performance device is more suited for use as a passivation material only rather than a gate dielectric/passivation combination.

II. Materials and Methods

A. Sample Fabrication and Characterization

A silicon wafer with pre-grown silicon oxide (1µm thick) and silicon nitride (100nm thick) is etched to create 500 nm deep trenches, and 500nm-2µm wide, depending on the desired device channel length. Platinum electrodes are patterned lithographically on top of the silicon nitride for source and drain formation, and in the middle of the trench for gate formation. Catalyst windows are patterned on top of the source and drain electrodes in order to allow iron catalyst deposition. Individual nanotubes are grown at temperatures between 800-900 °C The estimated diameter of CNTs grown using this method is 1-2nm [37]. During the nanotube growth, a mixture of argon bubbled in ethanol and hydrogen are fed into the furnace tube. The nanotube growth is carried out for 10 minutes. We pre-select the devices based on their I-V_g characteristics, as described previously [12, 30, 36].

B. *Pre-passivation Gate Voltage Sweeps*

Drain current versus gate voltage (I-V_g) characteristics were measured before and after parylene deposition for both semiconducting and metallic CNTFETs by sweeping the gate voltage from -3 to 3 V while maintaining the drain voltage at 100 mV and source voltage at 0 V. Measurements were performed by an Agilent 4155C semiconductor parameter analyzer in conjunction with a Cascade Microtech Summit probe station. Current was then measured through the drain during the sweep. Measurements were made at room temperature and atmospheric pressure in air.

C. *Parylene Deposition*

After the pre-passivation gate voltage sweeps were made, the samples were prepared for parylene deposition. Parylene deposition was accomplished using Specialty Coating Systems PDS 2010 LABCOTER™ 2. Samples with both 2 and 4 g of parylene-C were tested to give varying coat thicknesses. The recommended temperature and pressure set points were used (vaporizer at 175 °C, pyrolysis at 690 °C, and pressure at 35 vacuum units). Coat thicknesses are dependent on the surface area in the chamber, but no more than two samples (1 cm^2) were coated at a time so thickness differences between identical runs were negligible.[23] Parylene layer thickness is estimated to be 0.5 µm or 1 µm corresponding to the amount of parylene-C used.

D. *Post-passivation Gate Voltage Sweep*

After the parylene was deposited onto the CNTFETs, post-passivation I-V_g sweeps were performed on the same devices. Environment, gate, drain, and source voltages were kept the same as pre-passivation but small pockets on the contact pads had to be made by puncturing the parylene film using the probe tips to make electrical contact.

E. *Post-passivation Drain Voltage Sweeps*

Drain current versus drain voltage (I-V_d) sweeps were performed on a few of the devices to observe the effect of excessive heating of the CNT from using higher drain-source voltages. Drain voltage sweeps were taken with increasing drain voltage ranges. Gate voltages were set at -3 or -5 V with the source voltage kept at 0 V. Drain voltage ranges started from -0.2 V to 0.2 V and increased in increments of 0.4 V (-0.4 to 0.4 V, -0.6 to 0.6 V, etc.). If the resultant I-V_d curve changed, multiple sweeps would be run and averaged together to ensure the change was not transient. Before sweeps began, the probe station was purged of oxygen by continuously flowing N2 gas through the chamber for at least 20 minutes before, and during measurements. In between each drain voltage sweep, an I-V_g sweep was taken to observe the effect of the I-V_d sweep. Gate voltage sweeps were taken in the same way as mentioned above except that the sweep range was from -10 to 10 V.

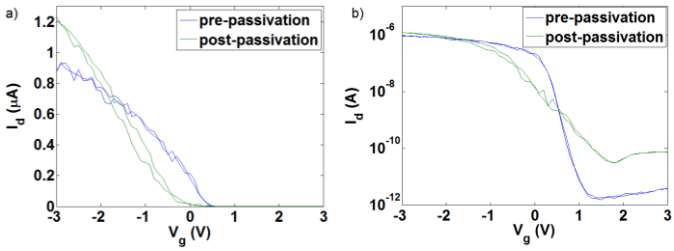

Fig. 2. I-V_g characteristic plot (V_d = 0.1V) of the same CNTFET before and after parylene deposition (linear (a) and log (b)). Note negligible hysteresis along with the clear changes in threshold voltage, On/Off ratio, Off current, and subthreshold swing.

F. *Analysis*

All data analysis on the I-V_g curves was done using MATLAB. Six parameters were calculated including hysteresis width, Off current, threshold voltage, On/Off ratio, subthreshold swing, and transconductance. Hysteresis was calculated by taking the drain current at each gate voltage in the forward sweep and interpolating the gate voltage in the backward sweep at the same current. The hysteresis width was defined as the difference in forward and backward sweep voltage. All other parameters were calculated after averaging the forward and backward sweeps. Off current was defined as the average current at all voltages above the voltage corresponding to the smallest current. On current was defined as the maximum current measured over the gate voltage interval. Threshold voltage was defined as the voltage at which the current was one-tenth of the maximum current. On/Off ratio was defined as the ratio between the maximum On and Off current. Subthreshold slope was calculated by finding the minimum slope in a semi-log curve. Finally, transconductance was defined as the minimum slope at voltages more negative than the threshold voltage.

III. Results

I-V_g characteristics (Figure 2) of 16 semiconducting CNTFETs pre- and post-passivation were analyzed using six parameters: hysteresis width, subthreshold swing, Offcurrent,On/Off ratio, threshold voltage, and transconductance (Figure 3, 4). All testing was done pairwise because of the differences between individual devices. Due to the presence of outliers and potentially non-normal distribution, interval hypothesis testing may not be most accurate [38]. Therefore, both paired t-tests (comparing means) and Wilcoxon signed-rank tests (comparing medians) were performed on the parameters. Three parameters showed statistically significant ($p < 0.05$) shifts in both tests: subthreshold swing,On/Off ratio, and threshold voltage. Off current and transconductance showed significant differences under the Wilcoxon signed-rank test while hysteresis width change was not significant under either test. Pairwise shifts were calculated as either ratios (after/before) for swing, Off current,On/Off ratio, and transconductance, or differences (after – before) for threshold voltage and hysteresis width. The overall shift was computed as the mean of the pairwise shift for each device after significant outliers (in Off current andOn/Off ratio) were removed (Table 1).

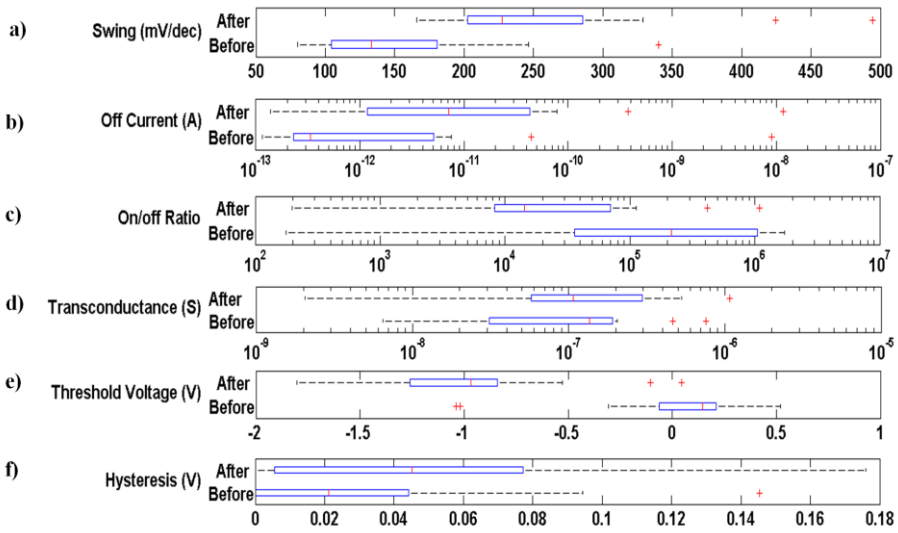

Fig. 3. Box plots of changes in electrical characteristics before and after passivation for 16 devices. a) swing, b) Off current, c) On/Off ratio, d) transconductance, e) threshold voltage and f) hysteresis width. Left and right box edge mark first and third quartiles. Middle red line marks the median. Outliers are marked as red crosses.

Hysteresis was found to be negligible (mean width < 0.2 V) both pre- and post-passivation in all of the transistors measured. Hysteresis in CNTs is thought to occur due to the interfacial defects between the CNT and gate dielectric and bulk defects in the dielectric itself leading to charge injection and trapped charges [39, 40]. The lack of hysteresis before passivation can be attributed to the use of suspended pristine CNTs without a gate dielectric to form significant defects. After passivation the hysteresis did not significantly increase even though sweep measurements were done immediately, implying that the number of defects in the parylene and CNT-parylene interface did not increase significantly.

All of the other parameters show significant shifts after parylene passivation. Previous research has shown that substrate-CNT interactions can cause trapped charges and additional interface states around the channel [41, 42]. These changes could be caused by diameter-dependent s-p hybridization between the parylene and CNT leading to a shift in charge distributions [41]. The charges trapped inside of the parylene as more sweeps were run could have also led to degrading characteristics. Increased charge traps have been shown to lower subthreshold slope [43] and threshold voltage [39]. This interaction with the substrate and associated charge traps and interface states has also been shown to yield inhomogeneous broadening of the Fermi energy in CNTs, leading to higher Off currents and subsequently lowerOn/Off ratios [30].

I-V_d (V_g = -5 V) sweeps pre- and post- parylene passivation of metallic CNTFETs show an increase in current after passivation. This is attributed to increased dissipation of thermal energy to the environment due to heat conduction through the surrounding parylene coating. The *I*-V_d curves also show that slight negative differential conductance (NDC) is observed pre-passivation. The NDC is thought to be caused by the combined effects of self-heating and optical phonon emission, causing backscattering at high fields [44, 45]. Post-passivation, this phenomenon disappears, corroborating the evidence in dry-ice coated CNTs from Mann et al. [46] This

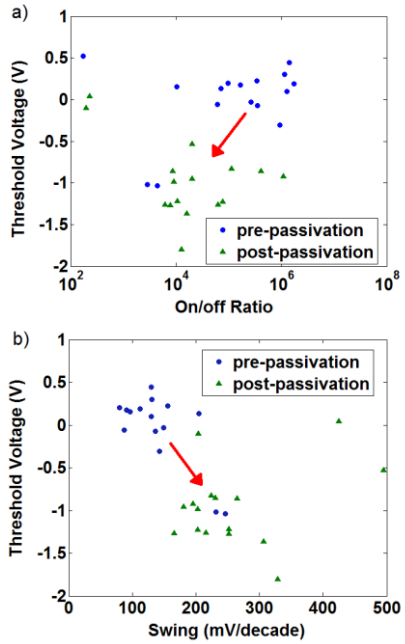

Fig. 4. Scatter plot of a) On/Off ratio versus threshold voltage and b) subthreshold swing versus threshold voltage both pre- and post-parylene passivation, showing a shift to higher swing, lower threshold voltages, and lower On/Off ratio.

further reinforces the finding that adsorbed molecules on the surface of the CNT can couple to hot optical phonons at high drain voltages and relax them, allowing for higher currents and elimination of NDC (Figure 5).

Drain voltage sweeps (V_g = -3 V) of the parylene-coated semiconducting 500 nm channel length CNTFETs show that the CNTFETs behave normally until a drain voltage of about 2 V. Subsequent *I*-V_g curves sh ow negligible change while the drain voltage is kept below 2 V. However, when the drain voltage sweep exceeds a ±2 V range, both the drain voltage and gate voltage sweeps show changes (Figure 6). Figures 6a and 6b show the effect of high drain voltage sweeps on drain and gate voltage sweep shape. Figures 6c – 6g show the effect

TABLE I
ELECTRICAL CHARACTERISTICS BEFORE AND AFTER PARYLENE PASSIVATION

Electrical Parameters		Subthreshold Swing (mV/dec)	Off Current (A)	On/Off Ratio (A/A)	Trans-conductance (S)	Threshold Voltage (V)	Hysteresis Width (V)
Before	Mean	154	5.70E-10	4.92E+05	1.63E-07	-0.005	0.0317
	Median	133	3.35E-13	2.16E+05	1.35E-07	0.145	0.00212
After	Mean	259	7.69E-10	1.15E+05	2.25E-07	-0.961	0.0542
	Median	227	7.09E-12	1.44E+04	1.06E-07	-0.968	0.0452
Pairwise Shift		1.84	12.3	0.223	1.33	-0.956 V	0.0224 V

Table 1. Results of the MATLAB analysis for the six parameters showing the mean and median data before and after parylene deposition. The pairwise shift shows the mean or median ratio (after/before) for swing, off current, on/off ratio, and transconductance and shows the difference (after – before) for the threshold voltage and hysteresis width.

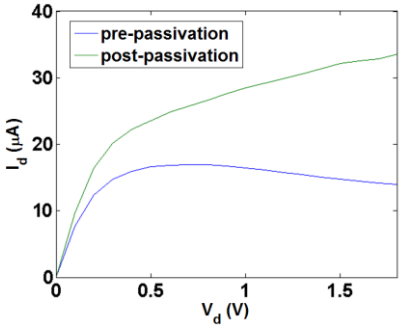

Fig. 5. Drain voltage sweep (V_g = -5 V) of a metallic CNTFET before and after passivation showing the elimination of negative differential conductance (NDC) and higher currents.

of high drain voltages on the fit values of threshold voltage,On/Off ratio, subthreshold swing, Off current, and transconductance (respectively) extracted from the I-V_g curves. The gate voltage sweep shows that the threshold voltage starts to decrease along with theOn/Off ratio. On the other hand, the swing continues to increase while the Off current and transconductance is largely not affected. Drain voltage sweeps also reflect these changes by the delayed increase in current until higher and higher drain voltages. Interestingly, when the same set of I-V_d sweeps were performed with a positive gate voltage (V_g = 5 V), all the I-V_g characteristics degraded with higher drain voltages, however the threshold voltage did not shift at all. This continued degradation and threshold voltage shift with negative gate voltages sweeps points to hot carrier injection leading to further increased charge trapping as more holes are bound to the interface [42].

IV. CONCLUSION

In conclusion, we demonstrated a simple passivation process for CNTFETs using parylene-C that allows for both use in integrated electronics as well as flexible electronics. Using this process, we were able to perform the first comprehensive analysis of the electrical characteristics of individual suspended single-walled CNTFETs showing the changes before and after parylene passivation. There was no significant hysteresis observed before or after passivation, avoiding the problem observed in most CNTFET devices. All of the other parameters (subthreshold swing, Off current,On/Off ratio, transconductance, and threshold voltage) compared showed statistically significant shifts from before and after passivation. Device operation was preserved after parylene passivation, however most of the observed changes were moderately unfavorable. On/Off ratios were as high as

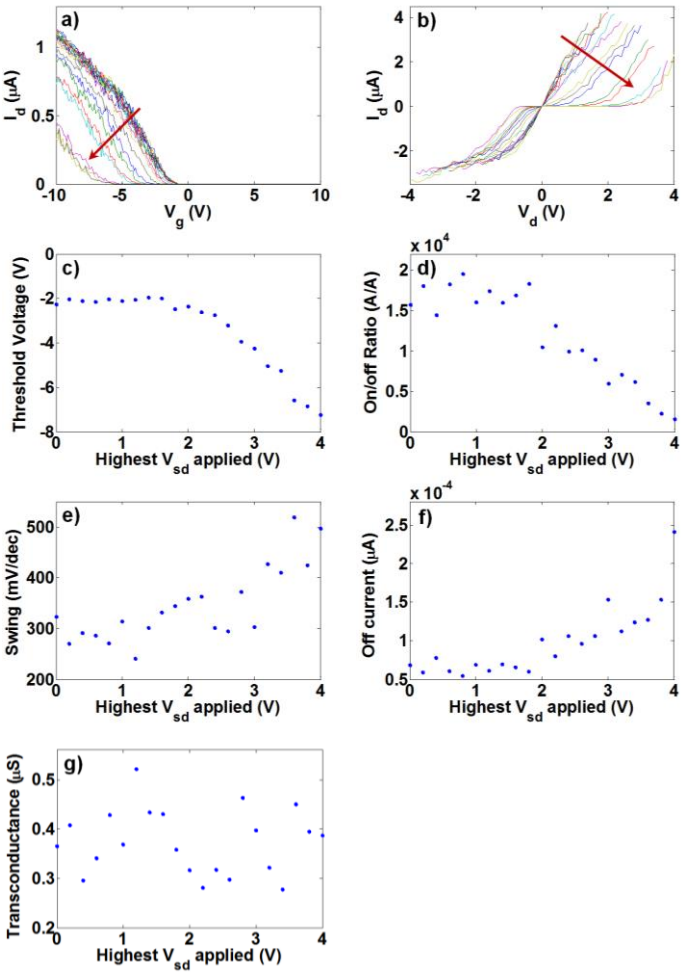

Fig. 6. Gate (V_d = 0.1V) and drain (V_g = -3 V) voltage sweeps of a 500 nm channel semiconducting CNTFET. Gate voltage sweeps are shown in a) with the preceding drain voltage sweep shown in b) ranging from 0.2 V to 4 V in 0.2V increments. Analysis of the gate voltage sweeps show that the c) threshold voltage, d) On/Off ratio, e) and subthreshold swing all change starting after about 2 V drain voltage sweep. Each data point in c) - g) corresponds to one I-V sweep in a) and b). The swing increases while the On/Off ratio and threshold voltage decrease linearly after a highest V_d of 2 V. f) Off current and g) transconductance current show minimal change throughout the sweep.

10^5 after passivation, whileOn-current remained equal or increased slightly. Transconductance increased marginally retaining its usefulness in both analog and digital applications. While more research still needs to be done to better understand the physics behind these electrical changes, here we have shown that parylene-C can serve as a viable passivation layer for CNTFETs.

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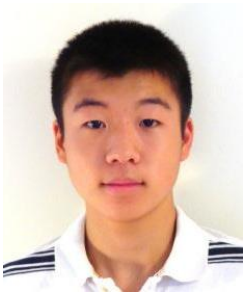

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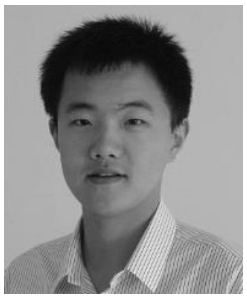

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