Electrical Transport and Channel Length Modulation in Semiconducting Carbon Nanotube Field Effect Transistors

Adam W. Bushmaker, Moh. R. Amer, and Stephen B. Cronin

***Abstract*—We perform finite-element analysis modeling and characterization of quasi-ballistic electrical transport in semiconducting carbon nanotube field effect transistors, and fit experimental electrical transport data from both suspended and on-substrate single-walled carbon nanotube transistors fabricated using chemical vapor deposition. Previous studies have focused on modeling ballistic transport in carbon nanotube field effect transistors, but have ignored the spatial dependence of the resistance, voltage, and Fermi energy. These spatial variations play an important role in several high voltage effects that are particularly important in the quasi-ballistic transport regime where most current or near-term devices operate. We show the relationship between device geometry and pinch-off, current saturation, and channel length modulation in the quantum capacitance regime. Output resistance is found to increase with gate coupling efficiency with a power law behavior. This model can be used for the extraction of device properties from experimental data and as a design environment tool.**

***Index Terms*—Carbon nanotube (CNT), finite-element methods, semiconductor device modeling, transistors.**

I. Introduction

SINGLE-WALLED carbon nanotube (CNT) field-effect transistors (FETs) are unique devices because of their intrinsically one-dimensional (1-D) transport, tunable band gap, and high mobility. They also offer potential performance advantages such as high-linearity in analog RF amplifiers [1], high surface-to-volume ratio, which is useful for chemical sensors [2], high-frequency mechanical oscillations for RF NEMs devices [3], and high cutoff frequencies in the terahertz region [4]. Several research groups have used theoretical and computational methods to analyze electrical transport in CNT FETs [5], [6], most notably Datta *et al.* [7], [8]. Several software tools for performing these simulations are available on the nanoHUB.org website, such as the FETToy tool [9]. Some studies have focused on improving numerical methods [10], [11], whereas other researchers have focused on modeling of CNT FETs for process design guidance [12] and circuit design [13]. Several studies have emphasized specific aspects of transport in CNT FETs, such as multiband mobility [14], carrier velocity saturation [15], Shottky barrier effects [16], and electron-phonon scattering [17], [18]. These studies and tools, however, all assume a uniform voltage, resistance, and Fermi energy along the length of the CNT. For ballistic transport, this assumption is not valid because the gate, source, and drain capacitances vary spatially, and this requires a spatial solution of Poisson's equation to obtain the voltage and carrier number density distribution. In devices that experience quasi-ballistic and diffusive transport, this approximation precludes modeling of pinch-off and channel length modulation, effects that strongly influence electrical transport in FET devices. Here, we perform numerical modeling of electrical transport in CNT FETs within the Landauer framework, while explicitly including spatial inhomogeneity by calculating the voltage, resistance, and Fermi energy at discrete points along the CNT channel, a technique known as finite-element analysis. Such analysis is urgently needed in order to examine the dynamics of the pinch-off and channel length modulation, both of which are useful to gain a complete understanding of CNT FET operation and as a design tool for device processing optimization and CNT-based circuitry.

II. Device Fabrication and Experimental Details

In order to validate the results from the model outlined in the body of this paper, experimental data from suspended CNT FETs fabricated using chemical vapor deposition (CVD) are compared with output from the model. These samples are fabricated as reported previously [19], [20] on pre-defined platinum/tungsten electrode structures. Fig. 1 shows scanning electron micrograph (SEM) images of a CNT FET device fabricated using this method. The CNT is grown in the CVD process across a trench etched in the underlying substrate, making electrical contact on both sides of the trench. The trench has a metallic top layer that serves as a gate electrode, with the ambient gas or vacuum serving as the dielectric between the CNT and the gate. The yield is low ($\sim$5%), and devices with CNTs successfully spanning the trench are selected for further study. The CVD process is the last step in fabrication, ensuring low-defect concentration in the resulting CNT channel material.

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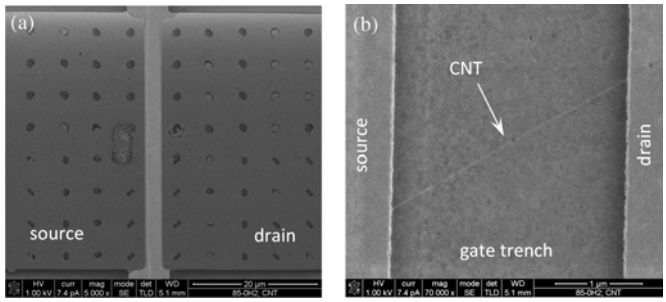

Fig. 1. CNT device geometry. (a) SEM images of CNT device layout and (b) close-up image of a single CNT crossing the trench.

III. Computational Model

In the Landauer model, electrical current flowing in a ballistic 1-D conductor is

$$\boldsymbol{I} = \int_{-\infty}^{\infty} \boldsymbol{D}\left(\boldsymbol{E}\right) \cdot \boldsymbol{v_g}\left(\boldsymbol{E}\right) \left[\boldsymbol{f_R}\left(\boldsymbol{E}\right) - \boldsymbol{f_L}\left(\boldsymbol{E}\right)\right] \boldsymbol{dE} \quad (1)$$

where $v_g\left(E\right)$ is the group velocity, $D\left(E\right)$ is the density of states, and f_R and f_L are the quasi-Fermi functions for the right and left moving electron populations. From this equation, the resistance $\boldsymbol{R}_s$ of a diffusive CNT section "s" of length L can be approximated [14], [21] as

$$\boldsymbol{R_s} = \boldsymbol{R_0 L} / \int_{\mathbf{bands}} \boldsymbol{\lambda}\left(\boldsymbol{E}\right) \left(\frac{-\boldsymbol{df}\left(\boldsymbol{E}\right)}{\boldsymbol{dE}}\right) \boldsymbol{dE} \quad (2)$$

where $R_0 = h/4e^2$ is the quantum resistance, λ is the mean free path, f is the Fermi function for the average Fermi energy $E_F = \left(E_{F,R} + E_{F,L}\right)/2$, and the integral is taken over all energies except the band gap, i.e, $\int_{\mathbf{bands}} \boldsymbol{dE} = \int_{-}^{E_v} \boldsymbol{dE} + \int_{E_c}^{\infty} \mathbf{dE}$. For multiple sections of one dimensional conductor in series with one another, the resistance can be calculated as

$$\boldsymbol{R} = \boldsymbol{R_0^*} + \boldsymbol{\Sigma R_s} + \boldsymbol{2R_C} \quad (3)$$

where

$$\boldsymbol{R_0^*} = \boldsymbol{R_0} / \int_{\mathbf{bands}} \left(\frac{-\boldsymbol{df}\left(\boldsymbol{E}\right)}{\boldsymbol{dE}}\right) \boldsymbol{dE} \quad (4)$$

is the *depleted* quantum resistance evaluated at the point of minimum doping on the CNT, and R_C is the contact resistance. If $\lambda \gg L$ (ballistic transport), the right-hand side of (3) reduces to the depleted quantum resistance plus the contact resistances. The mean free path λ is, is given by

$$\boldsymbol{\lambda} = \left(\mathbf{1}/\boldsymbol{\lambda_{ac}} + \mathbf{1}/\boldsymbol{\lambda_{op,ems}}\right)^{-1} \quad (5)$$

where λ_{ac}, the mean free path for electron scattering by acoustic phonons, is given by

$$\boldsymbol{\lambda}_{\mathrm{ac}}\left(\boldsymbol{E}\right) = \boldsymbol{\lambda}_{\mathbf{ac}}^{\mathbf{high}\boldsymbol{E}} \left(\frac{v_g\left(E\right)}{v_F}\right)^2 \quad (6)$$

where $\lambda_{\mathrm{ac}}^{\mathrm{high}E}$ is the mean free path at high energies away from the band edge, and v_F is the carrier velocity in graphene. Acoustic scattering is approximated as elastic as in [14]. A more complete discussion of electrical transport modeling with inelastic scattering accounted for can be found elsewhere [22]. The mean free path is related to the scattering rate $\tau^{-1}\left(E\right)$ according to $\lambda_{\mathrm{ac}}\left(E\right) = \tau\left(E\right) * v_g\left(E\right)$. Because the scattering rate increases with the density of states (Fermi's golden rule) near the band edge, $\tau^{-1}\left(E\right) \propto D\left(E\right) \propto v_g^{-1}\left(E\right)$. A full derivation of this effect is beyond the scope of this paper, but the divergence of the scattering rate at the band edge where the group velocity goes to zero can be seen elsewhere in the carbon nanotube literature [23]–[25]. The combined effect gives a mean free path proportionate to v_g^2. The energy dependence of λ_{ac} is thermally averaged, but still varies by a factor of 5 or so at room temperature as the Fermi energy is changed. Electrons in 1-D systems scatter strongly from with K-point optical phonons [26]. The mean free path with respect to electron scattering through optical phonon emission $\lambda_{\mathrm{op,ems}}$ is given by

$$\boldsymbol{\lambda}_{\mathbf{op,ems}} = \frac{\boldsymbol{E_{op}L}}{\boldsymbol{qV}} + \boldsymbol{\lambda}_{\mathbf{op,min}} \quad (7)$$

where V is the voltage drop across the segment, $\lambda_{\mathrm{op,min}}$ is the scattering length for electrons with enough energy to emit an optical phonon, and $E_{\mathrm{op}} = 0.16\mathrm{eV}$ is the optical phonon energy of the zone-boundary optical phonons [26]. The voltage drop in (7) approximates the Pauli exclusion factor $1 - f\left(E - E_{\mathrm{op}}\right)$. This relationship was discussed by Park *et al.* [26], and can be justified because $k_B T \ll E_{\mathrm{op}}$. The temperature dependence for the quantities in (5)–(7) can be found elsewhere in the literature [27]. The voltage $V\left(x\right)$ and $E_F\left(x\right)$ at given section along the CNT can be calculated by solving Poisson's equation [7] to obtain (8), as shown at the bottom of the page, where V_G is the gate voltage, $C_\Sigma = C_G + C_s + C_d$ is the net capacitance from the section of the CNT to the gate, source and drain contacts, and

$$\boldsymbol{Q}\left(\boldsymbol{E_F}\right) = \int_{-\infty}^{0} \left[\mathbf{1} - \boldsymbol{f}\left(\boldsymbol{E}\right)\right] \cdot \boldsymbol{D}\left(\boldsymbol{E}\right) \boldsymbol{dE} - \int_{0}^{\infty} \boldsymbol{f}\left(\boldsymbol{E}\right) \cdot \boldsymbol{D}\left(\boldsymbol{E}\right) \boldsymbol{dE} \quad (9)$$

is the linear charge density on the CNT section. The main effect of the source and drain capacitances is to screen the influence of the gate near the contacts. We can make the approximations $C_s\left(x\right) = C_{sd0}\frac{x_d}{x}$ and $C_d\left(x\right) = C_{sd0}\frac{x_d}{x_d - x}$, which were validated by an electrostatic finite-element analysis of a standard

$$qE_F\left(x\right) = \frac{Q\left(E_F\left(x\right)\right) + \left(V_G - V\left(x\right)\right) C_G + \left(V_s - V\left(x\right)\right) C_s\left(x\right) + \left(V_d - V\left(x\right)\right) C_d\left(x\right)}{C_\Sigma} \quad (8)$$

FET device geometry in Comsol Multiphysics software package. In this model, C_{sd0} is a characteristic capacitance per unit length for the source-channel and drain-channel capacitances x_d is the source-drain separation, and C_0 is the gate capacitance per unit length. Furthermore, we can say that $V_s = \Delta\mu$ and $V_d = \Delta\mu + V_T$, where $\Delta\mu$ is the surface potential of the contact metal relative to the CNT, and V_T is the voltage drop across the CNT.

The contact capacitances C_s and C_d become very large near the contact. When they become significantly larger than both the quantum capacitance and the gate capacitance, (8) dictates that $E_F = \Delta\mu$, fixing the CNT Fermi energy at the contact. This can create a Schottky barrier, and describes the contact doping responsible for n/p-type operation in CNT FETs [28]. This energy difference is not simply the work function difference between the CNT and the metal; complex surface interactions can introduce deviations from this value [29]. In order to solve this equation, $E_F(x)$ and $Q(x)$ are solved for $V(x)$ numerically with (9) by use of a lookup table. By making the approximation $V(x) = \frac{x}{x_d} V_T$ and substituting into (8), one obtains

$$\boldsymbol{qE_F} = \frac{Q(E_F) + \Delta\mu(C_s + C_d) + (V_G - V(x))C_G}{C_\Sigma}. \tag{10}$$

This approximation assumes a linear voltage drop along the CNT, and as such, fails to include the effects of pinch-off and channel length modulation, which give rise to finite output resistance in the saturation region. The density of states $D(E)$ is given by

$$\boldsymbol{D}(\boldsymbol{E}) = \frac{dk}{dE}\frac{L}{\pi} \tag{11}$$

where $k(E)$ is the wavenumber in the hyperbolic band structure, given by

$$\boldsymbol{k}(\boldsymbol{E}) = \frac{1}{\hbar v_F}\left|\sqrt{\boldsymbol{E}^2 - \left(\frac{E_g}{2}\right)^2}\right| \tag{12}$$

where $v_F = 840\,000\,^{\mathrm{m}}/_{\mathrm{s}}$ is the Fermi velocity of graphene, and E_g is the band gap.

The subthreshold slope S is related to the gate efficiency according to

$$\boldsymbol{S} \cong \frac{kT}{q}\frac{1}{\mu}\ln(\mathbf{10}) \tag{13}$$

where $\alpha = \frac{C_G}{C_{\Sigma\min}}$ corresponds to the gate efficiency of the segment with the most efficient gate capacitance (the least contact screening). In the simplistic model for the contact capacitance outlined above, $C_{\Sigma\min} = C_G + 4C_{sd0}$. The voltage drop in each section of the CNT is $\Delta V = I_d R_s$, where I_d is the drain current. In order to perform the complete calculation for the electrical conductivity using the equations above, the device parameters needed are $E_g, R_C, \lambda_{\mathrm{ac}}^{\mathrm{high}E}, \Delta\mu, C_0, \alpha$, and x_d. Given experimental data from a CNT FET device, it is possible to use the equations above in a fitting exercise to extract these parameters from the device. If one or several of these parameters are known *a priori*, e.g., from device dimensions, the others can be determined with greater confidence. Also, since the relevant physics of electrical transport are being considered, these equations allow for realistic modeling of devices with known parameters in a design environment.

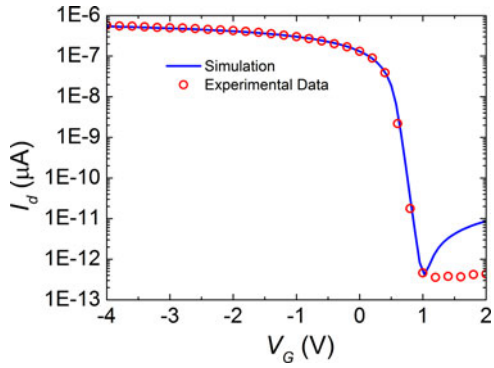

Fig. 2. Low voltage electrical transport data. Drain current versus gate voltage for a semiconducting CNT. Experimental data (red circles) and theoretical transport model (blue line) agree nicely for $V_G < 1$ V.

For small V_{sd}, the current and spatial voltage profile of the CNT are calculated for a given V_{sd} by iteratively solving the above equations. This approach follows the general scheme: guess $V(x)$ for all x, calculate $R(x)$, calculate $V(x)$ again, and iterate until convergence is reached. For V_{sd} high enough to induce current saturation, however, this algorithm is problematic, because for each iteration, the calculated drain current I_d changes, which results in a change in $V(x)$ and the effective gate voltage, creating an unstable feedback loop. Furthermore, for $|V_{sd}| > |V_G - V_{\mathrm{th}}|$, parts of the CNT become completely depleted in a "super pinch-off" condition, and the simulation produces a curve that exhibits negative differential resistance, which is not observed in field effect transistors affected by pinchoff alone (i.e., without self-heating [27]). This instability is mitigated by calculating $V(x)$ for a fixed I_d and V_d, and using an error minimization algorithm to adjust I_d until $V(x_d) = V_d$. This creates a spatial source-drain causality, where the voltage of any given element is only affected by elements to one side. This procedure is more computationally intensive, but can still be run on an office laptop computer.

IV. Results

Fig. 2 plots experimental data (red dots) taken from an isolated, suspended, semiconducting CNT FET showing drain current plotted as a function of gate voltage. The device is modeled as a p-type, with high on-current at negative gate voltages, an ON–OFF ratio of approximately 1×10^6, and a subthreshold slope of ~100 mV/decade. Plotted along with the experimental data is a curve calculated using Landauer transport theory (blue line). In order to fit the data, the simulation parameters are, gate capacitance $C_G = 10$pF/m, gate coupling efficiency $\alpha = 62\%$, high energy mean free path $\lambda_{\mathrm{ac}}^{\mathrm{high}E} = 1100$ nm, band gap $E_g = 0.85$ eV, and contact resistance $R_C = 60$ kΩ. The CNT channel length was set at $x_d = 1$ μm, in accordance with the actual device geometry. For $V_G > 1$V, the theoretical model does not agree well with the experimental data. Here, the CNT FET undergoes bipolar transport (diode behavior, with p-type contacts and n-type channel), which is not considered by the model. A

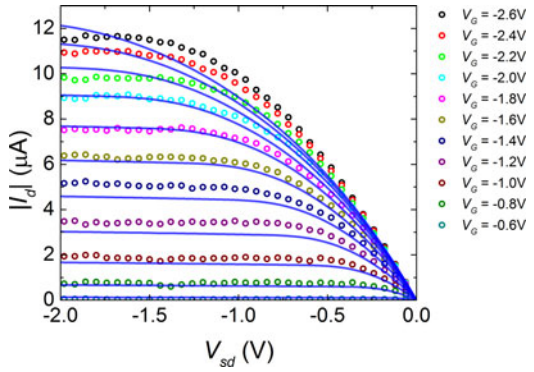

Fig. 3. High voltage electrical transport data. Experimental (open circles) and theoretical (blue lines) drain current plotted versus source-drain voltage for various gate voltages. The experimental data is from [25] (reprinted with permission).

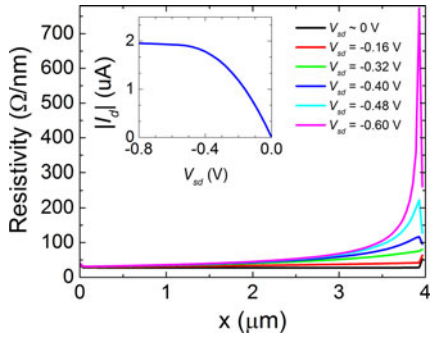

Fig. 4. Pinchoff in a CNT FET. Resistivity versus spatial position along the length of a CNT FET during development of the pinchoff condition. Inset shows drain current versus source-drain voltage for this calculation.

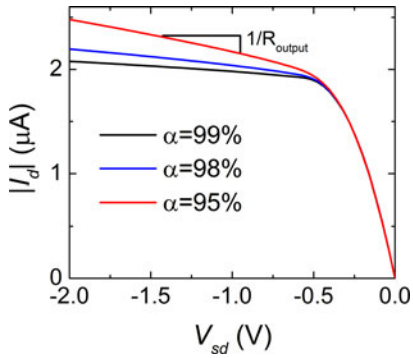

Fig. 5. Channel length modulation in a CNT FET. Drain current versus source-drain voltage at gate efficiencies α of 99%, 98%, and 95%, showing decreased output resistance for lower gate coupling efficiencies caused by channel length modulation.

further discussion of electrical transport can be found elsewhere in the literature [30], [31].

Fig. 3 shows a curve manifold containing experimental I_d versus V_{sd} data measured from a substrate-bound CNT FET from [32] (reprinted with permission), fabricated with HfO_2 gate dielectric and Pd contact electrodes. Zhang *et al.* state that the channel length was 4 μm, the diameter 2 nm, and the gate capacitance 150pF/m. The *I–V* curves were measured at a variety of gate voltages from -2.6 to -0.6 V, and are plotted along with simulation results from the theoretical model outlined here. The device is p-type, with larger conductance at negative gate voltages. The behavior is Ohmic at low voltages before transitioning into the saturation region. The simulation parameters were manually adjusted until a reasonable fit was achieved. The simulation parameters are, gate capacitance $C_G = 120$pF/m, gate coupling efficiency $\alpha = 99\%$, high energy mean free path $\lambda_{\rm ac}^{{\rm high}E} = 580$ nm, band gap $E_g = 0.42$ eV, contact resistance $R_C = 3.96$ kΩ, values which agree reasonably well with the experimental device parameters. The CNT channel length was set at $x_d = 4\mu$m, in accordance with the value reported by Zhang *et al.* The fitting parameters introduced here are the minimum number of parameters necessary to capture the physics of channel length modulation in a CNT FET. Similar current saturation plots have been reported in the literature [32]–[37]. Due to the difficulty of fitting so many different data curves through trial and error, there is some deviation between the theoretical model and the experimental data. Most of the deviation is concentrated at large negative V_G and large V_{sd}, when the device is deep in the "ON" state. Despite these small deviations, the theoretical model fits the experimental data reasonably well. Computer automated error minimization algorithms could reduce this error; however such an investigation was beyond the scope of this study.

Fig. 4 shows the linear resistivity along the length of the CNT at selected V_{sd}, taken at a gate voltage of $V_G = -1$ V, for the same substrate-bound CNT FET of Fig. 3. The curves illustrate the pinchoff effect which is responsible for current saturation at high source-drain bias voltages. Near the drain electrode, the voltage drop along the CNT causes the effective gate voltage to be lowered, reducing the charge density in the pinchoff region, which becomes progressively more and more depleted of carriers. As a result, the resistivity in this region is large. The charge carrier densities in sections of the CNT channel to the left of the pinchoff region, however, remain relatively unchanged.

Fig. 5 shows drain current saturation curves for the same CNT FET with different values for gate efficiency α. For high gate efficiency (low channel-source and channel-drain capacitances), the output resistance is high with a finite output resistance in the current saturation region due to channel length modulation, caused by channel-drain capacitive coupling. For low gate efficiencies, however, the output resistance is low. From the equations above, the gate efficiency is described by $\alpha = C_G/(C_G + \frac{4C_{sd0}}{x_d})$.

The *I–V* curves shown in Fig. 5 were calculated for many different values of C_G, α, and V_G, and the slope of the current saturation region in the resulting *I–V* curves was fit to determine the output resistance as a function of the different variables, in order to examine the relationship between device geometry and pinchoff, current saturation, and channel length modulation. The range of gate capacitance modeled in the simulation includes values from 15 to 480 pF/m. This range was chosen deliberately to include values both above and below the theoretical quantum capacitance for a CNT of 96 pF/m [38], [39]. Fig. 6 shows $R_{\rm output}$ plotted versus $1-\alpha$ for different gate voltages, with $C_G = 15$ pF/m and gate voltage range –2.6 V $< V_G < -0.6$ V. The threshold voltage $V_{\rm th} \sim -0.6$ V. $R_{\rm output}$ displays a power law

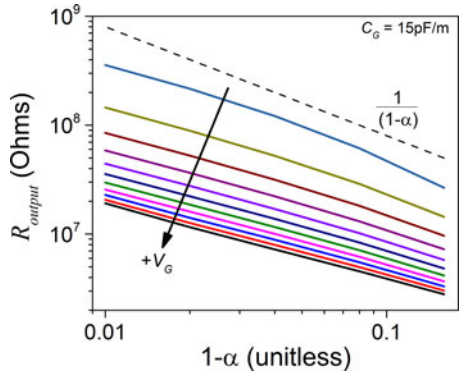

Fig. 6. Output resistance as a function of $1-\alpha$ for different gate voltages ($V_g = -2.6$ to -0.6 V). $R_{\rm output}$ has a power law dependence on $1-\alpha$, with $R_{\rm output}$ increasing as $\alpha \to 1$.

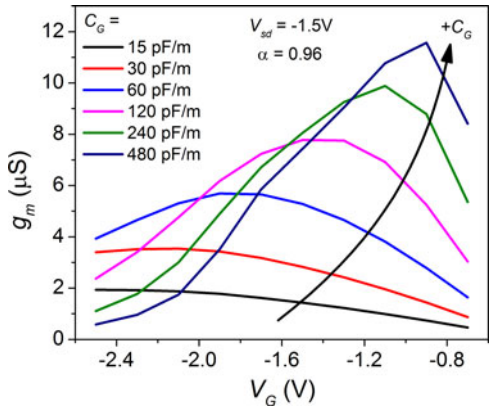

Fig. 7. Transconductance g_m versus gate voltage for several different gate capacitance values at a $V_{sd} = -1.5$ V and $\alpha = 96\%$.

dependence on $1-\alpha$ according to $R_{\rm output} \propto (1-\alpha)^p$ with $p = -0.93$ at $V_G \sim V_{\rm th}$ and $p = -0.69$ at $V_G = -2.6$ V. For higher gate capacitances, the value of p varies more widely. At $C_G = 480$ pF/m, $p = -1.0$ at $V_G \sim V_{\rm th}$ and $p = -0.38$ at $V_G = -2.6$ V.

From the numerical simulations, it is also possible to calculate the transconductance g_m for different transistor configurations in the current saturation regime. Fig. 7 shows the calculated g_m versus V_G for the same CNT FET with several different values of C_g, a gate efficiency $\alpha = 96\%$, and $V_{sd} = -1.5$ V. The transconductance peaks at different voltages for the different gate capacitances, with transconductance actually decreasing with increasing gate capacitance for $V_G < -1.6$ V. Possible causes for this could be saturation of the CNT channel for high carrier concentrations, or optical phonon emission onset at the high drain currents that accompany high carrier concentrations. g_m was also characterized with respect to the gate efficiency α, however it was found to vary very little with changes in α.

V. Conclusion

In conclusion, we have used the Landauer model used to calculate electrical transport in semiconducting carbon nanotube field-effect transistors at high source-drain voltages and for arbitrary gate voltages in the quantum capacitance limit. The model is used to fit experimental electrical transport data from suspended and substrate-bound single-nanotube CNT FETs. The model successfully reproduces the subthreshold slope, ON–OFF ratio, superthreshold roll-off, and current saturation at high voltage. The model captures the physics of the channel length modulation effect, which results in finite output resistance in FETs. This model is a useful tool in characterizing, predicting, and optimizing electrical performance of carbon nanotube field effect transistors for both digital and analog applications.

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