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Effects of basal-plane thermal conductivity and interface thermal conductance on the hot spot temperature in graphene electronic devices

David Choi,[1] Nirakar Poudel,[2] Stephen B. Cronin,[2] and Li Shi[1,3,a)]
[1]*Department of Mechanical Engineering, The University of Texas at Austin, Austin, Texas 78712, USA*
[2]*Department of Electrical Engineering, University of Southern California, Los Angeles, California 90089, USA*
[3]*Texas Materials Institute, The University of Texas at Austin, Austin, Texas 78712, USA*

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Electrostatic force microscopy and scanning thermal microscopy are employed to investigate the electric transport and localized heating around defects introduced during transfer of graphene grown by chemical vapor deposition to an oxidized Si substrate. Numerical and analytical models are developed to explain the results based on the reported basal-plane thermal conductivity, κ, and interfacial thermal conductance, G, of graphene and to investigate their effects on the peak temperature. Irrespective of the κ values, increasing G beyond $4 \times 10^7\,\mathrm{W\,m^{-2}\,K^{-1}}$ can reduce the peak temperature effectively for graphene devices made on sub-10 nm thick gate dielectric, but not for the measured device made on 300-nm-thick oxide dielectric, which yields a cross-plane thermal conductance (G_{ox}) much smaller than the typical G of graphene. In contrast, for typical G values reported for graphene, increasing κ from $300\,\mathrm{W\,m^{-1}\,K^{-1}}$ toward $3000\,\mathrm{W\,m^{-1}\,K^{-1}}$ is effective in reducing the hot spot temperature for the 300-nm-thick oxide devices but not for the sub-10 nm gate dielectric case, because the heat spreading length (l) can be appreciably increased relative to the micron-scale localized heat generation spot size (r_0) only when the oxide layer is sufficiently thick. As such, enhancement of κ increases the vertical heat transfer area above the gate dielectric only for the thick oxide case. In all cases considered, the hot spot temperature is sensitive to varying G and κ only when the G/G_{ox} ratio and r_0/l ratio are below about 5, respectively. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4976511]

Because of its high intrinsic electron mobility, mechanical strength, optical transmission, and thermal conductivity, the envisioned uses of graphene have grown rapidly since its successful exfoliation just over a decade ago.[1–3] In particular, graphene has been explored for use in electronic devices fabricated on not only silicon but also flexible substrates due to the unprecedented electronic properties and mechanical flexibility of the two-dimensional (2D) material.[4] While the thermal management of silicon nanoelectronic devices has remained a significant challenge due to the high power density and high operating temperature,[5,6] similar challenges have emerged for graphene electronic devices. For example, thermomechanical failures have already been observed in flexible graphene electronic devices due to the low thermal conductivities and glass transition temperatures of most flexible substrates.[4,7,8] In addition, physical defects such as rips, tears, and wrinkles are often introduced during the fabrication of these devices and can potentially result in local hot spots during operation.[9–12] Such hot spots in turn can significantly degrade their performance and reliability. The high basal plane thermal conductivity of graphene has been explored to address this and other challenges in thermal management.[13,14] However, it remains elusive whether the high basal plane thermal conductivity of graphene can lead to an added benefit of enhanced heat removal and reduced peak temperatures during operation despite its atomic scale thickness.[7] Because of the high surface to volume ratio of graphene, it is unclear whether the hot spot temperature is more sensitive to the thermal interface conductance (G) between the 2D atomic layer and the substrate than to the in-plane thermal conductivity (κ).[7,15]

In this work, we employ electrostatic force microscopy (EFM) and scanning thermal microscopy (SThM) techniques to identify defects in a graphene electronic device and analyze their effect on thermal performance with nanoscale resolution. A numerical electro-thermal analysis is further employed to correlate the measured hot spot temperature with the basal-plane thermal conductivity and the interface thermal conductance of graphene. The results show that a high κ value of graphene can effectively reduce the hot spot temperature, while the interface thermal resistance does not present a bottleneck in thermal dissipation for the measured graphene device fabricated on the 300-nm-thick SiO_2 dielectric of a silicon wafer. This finding is explained with the use of an analytical model, which reveals that the hot spot temperature can be decreased effectively by increasing G when G is not much larger than the cross-plane thermal conductance of the underlying dielectric layer and substrate, and by increasing κ when the heat spreading length is not much smaller than the localized heat generation spot size near the defect.

Figures 1(a)–1(d) show the atomic force microscopy (AFM), SThM, and EFM measurement results of a graphene device. The device is comprised of a $12.6 \times 10\,\mu\mathrm{m}^2$ graphene channel contacted by Cr/Pd electrodes, as illustrated in the schematic of Fig. 1(e). Graphene was grown at 1000 °C for 40 min on a copper foil by low-pressure chemical vapor deposition (LPCVD) at 1.3 Torr pressure with the use of CH_4 as the carbon feedstock. The large area graphene was

a)Author to whom correspondence should be addressed. Electronic mail: lishi@mail.utexas.edu

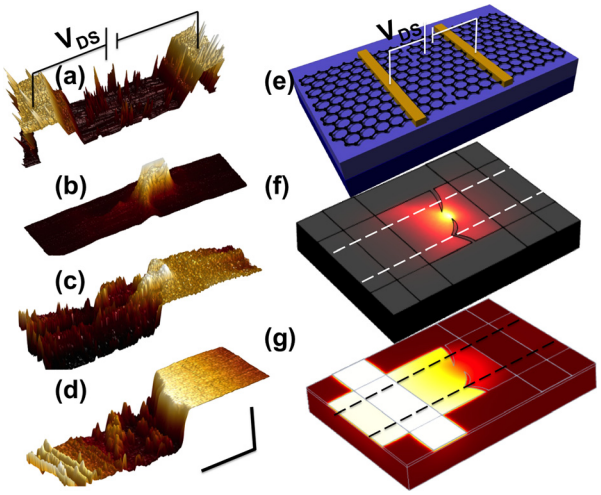

FIG. 1. Measured [(a)–(d)] and calculated [(f) and (g)] topographic (a), thermal [(b) and (f)], and electrical potential profiles [(c), (d), and (g)] of the graphene channel, which are illustrated in a schematic (e). (a) Three-dimensional (3D) AFM image showing the topography of device. (b) SThM image showing a localized hot spot. (c) EFM image showing a steep potential drop at the location where the hot spot is shown by the SThM image. (d) EFM image after the constriction is destroyed by ESD, showing a step change in the surface potential that spans the entire channel signifying an open circuit. Horizontal scale bar is 5 μm and the vertical scale bar is 50 nm, 160 K, 4° and 10° phase shift for images a, b, c, and d, respectively. (e) Schematic of device. (f) Numerical calculation results of the temperature distribution around a constriction in the graphene channel. The two white dashed lines enclose the area shown in the SThM image in (b). The color scheme reflects temperature, with lighter colors indicating higher temperatures. (g) The corresponding calculated electric potential distribution, where the black dashed lines enclose the area shown in the EFM image in (c). The color scheme reflects the electric potential, with lighter colors indicating a higher electric potential.

transferred to a Si substrate with a 300-nm-thick SiO_2 layer via a sacrificial polymethylmethacrylate (PMMA) transfer layer. The final rectangular graphene channel was then patterned by electron-beam lithography (EBL) and oxygen plasma etching. Electrodes and contacts were patterned by a second EBL step followed by evaporation of Cr (5 nm) and Pd (50 nm). The final device was annealed for 5 h at 500 °C in an inert argon ambient to decrease the PMMA residue on the graphene surface.

High-resolution surface temperature mapping was performed using a SThM probe consisting of a SiO_2 tip and a SiN_x cantilever.[16] A Pt-Cr thermocouple junction was fabricated on the tip with a final nominal radius of about 50 nm. Under ambient measurement conditions, conduction from the sample to the cantilever through air creates a non-local signal. This parasitic effect of the air was removed by a double scan technique reported in recent years.[8,17–19] During the first scan, the SThM tip profiles the surface in contact mode to obtain the sample topography and thermovoltage produced by the tip. In a second scan of the same line, the thermovoltage is recorded while the tip is lifted to a set height above the sample and traced along the stored topographic profile of the first pass. This non-contact thermal signal consists mostly of the component of conduction through the air gap. A 100 nm lift was used in this work. The sample temperature is related to the contact and lift measurement results according to

$$\Delta T_s = \beta(\Delta V_{CL}), \quad (1)$$

where ΔT_s is the surface temperature rise of the sample and ΔV_{CL} is the difference in the thermovoltage values measured during the contact and lift modes.[19] The factor β is directly related to the thermal contact resistance between the tip and sample surface and can be experimentally determined through calibration as described in prior reports.[8,19]

Figure 1(b) shows the measured temperature distribution on the graphene device when a 14 kW cm^{-2} dissipated power density was applied. For operating tear-free graphene devices measured in prior works,[8,19] the measured temperature profiles were smooth and diffuse within the channel, where a relatively large hot spot can exist because of non-uniformity in the local charge carrier density due to the variation in the gate field along the channel. Figure 1(b), in comparison, clearly shows a confined hot spot that is irregular in shape and concentrated in a very localized area. In addition, Figure 2 shows the experimental thermal profile through the center of the hot spot. The peak temperature rise was determined to be $\Delta T_{max} = 160 \pm 40$ K, which is more than one order of magnitude larger than for a defect-free graphene channel with a similar power density dissipation.[19]

To further examine the underlying cause of the observed hot spot in the graphene device, an EFM scan over the same channel was performed. The EFM probe (SCM-PIT, Bruker AFM Probes) consists of a Si tip on a Si cantilever. Electrical connectivity from the cantilever mount to the tip apex was established through a platinum-iridium coating. In a procedure similar to the non-contact SThM, EFM scans were performed in a lift mode to remove the topographical artifacts. An optimal lift height was determined by incrementally retracting the tip from the surface until the contact and lift scans showed a minimal correlation. Figure 1(c) shows a sharp potential drop down the center region of the channel with discontinuous steps in potential on either side of a constriction. The steep gradient within the narrow strip

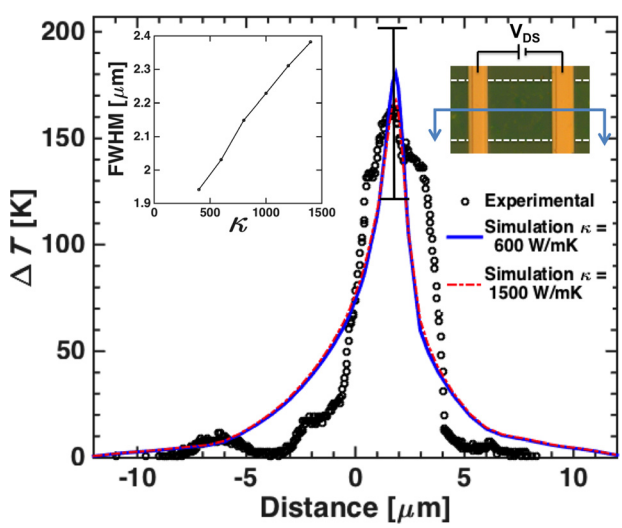

FIG. 2. Comparison of experimental (symbols) and simulation results (lines) for the centerline temperature profile through the channel. Numerical results plotted for $G = 9 \times 10^7$ W m^{-2} K^{-1}, $\kappa = 600$ W m^{-1} K^{-1} (blue solid lines) and $\kappa = 1500$ W m^{-1} K^{-1} (red dashed line). The left inset shows the increase of the full width at half maximum (FWHM) of the hot spot with increasing κ. The right inset shows an optical image of the device. The white dashed profile outlines the graphene channel, and the blue cross section indicates the location of the thermal profile shown in the figure.

of continuous graphene is coincident with and geometrically similar to the imaged hot spot, indicating the relation between the two.

The SThM and EFM results suggest the presence of a defect tear in the graphene, which creates the micro constriction in the channel. After the initial thermal and EFM scans were completed, the graphene channel was electrically broken by a large electrostatic discharge (ESD) current. Following this ESD, no current was observed upon application of a voltage bias to the channel. Figure 1(d) shows a potential discontinuity spanning the entire channel, confirming the breakage of graphene.

To better understand the experimental results, we have carried out a coupled electro-thermal transport simulation of the device. The geometry of the device, channel, and defect were reproduced in a numerical simulation through COMSOL Multiphysics with coupled electric and thermal transport equations. While the resistivity of electrically biased graphene has been shown to vary within the same channel, the resistance created by the experimentally observed narrow constriction is expected to be much larger than the variation due to the asymmetric distribution of charge carriers.[19] As such, an average graphene resistivity was specified to match the current resulting from the experimentally applied potential. Constant room temperature boundary conditions were specified on all lateral surfaces and the backside Si in the simulation domain. The thickness (t_{SiO_2}) and thermal conductivity (κ_{ox}) of the SiO_2 film under the graphene were taken to be 300 nm and $1.4\,W\,m^{-1}\,K^{-1}$, respectively. The thermal conductivity of the Cr/Pd line was calculated using the Wiedmann-Franz law and the measured four-probe electrical resistivity of the line.[19] Using the basal-plane thermal conductivity and interface thermal conductance values of $\kappa = 600\,W\,m^{-1}\,K^{-1}$ and of $G = 9.0 \times 10^7\,W\,m^{-2}\,K^{-1}$ reported in the literature for supported graphene,[20,22] the simulation predicts a $\Delta T_{max} = 180\,K$, which is within the uncertainty of the experimental results. This calculated profile is plotted with the experimental data in Fig. 2. The agreement suggests that the measured temperature rise can be explained with the literature κ and G values.

Much attention has been devoted to developing fabrication processes and identifying suitable support materials to achieve graphene basal plane thermal conductivities near its theoretical limit via reduction of defect and substrate scattering of phonons. However, it is unclear whether the atomic thinness of graphene limits its ability to conduct heat in the basal plane such that interfacial thermal transport is dominant compared to lateral heat spreading.[7] It has been proposed that the interfacial thermal conductance between graphene and substrate could become the bottleneck in heat dissipation.[15] A detailed analysis to examine the impacts of these two thermal properties on the hot spot temperature on graphene electronic devices would be useful.

Therefore, an extended numerical study of the effect of thermal conductivity and interfacial thermal conductance was performed. The calculated maximum temperature rise is plotted as a function of κ in Fig. 3(a) for increasing values of interfacial thermal conductance. Similarly, the inset shows the predicted maximum temperature rise as a function of G for increasing values of κ. Several important conclusions can be drawn from Fig. 3(a). The maximum hot spot temperature is very sensitive to the thermal interface conductance when G is low, and insensitive when the conductance is high. For any given κ, the gradient $\frac{\partial T_{max}}{\partial G}\big|_{\kappa}$ is large for $G \leq 4 \times 10^7\,W\,m^{-2}\,K^{-1}$ and drops thereafter. For example, at $\kappa = 600\,W\,m^{-1}\,K^{-1}$, increasing G from 1×10^7 to $2 \times 10^7\,W\,m^{-2}\,K^{-1}$ reduces the hot spot temperature by $40\,K$, whereas increasing G from 9×10^7 to $10 \times 10^7\,W\,m^{-2}\,K^{-1}$ only produces a 0.8 K reduction in maximum temperature. This behavior can be seen more clearly in the inset of Fig. 3(a), where the effect of increasing G on ΔT_{max} quickly saturates, regardless of the graphene thermal conductivity.

In contrast to the interfacial conductance, reductions in ΔT_{max} do not saturate appreciably with increasing thermal conductivities. Within the range $300 < \kappa < 1200\,W\,m^{-1}\,K^{-1}$, a maximum drop of ΔT_{max} from 565 K to 525 K can be

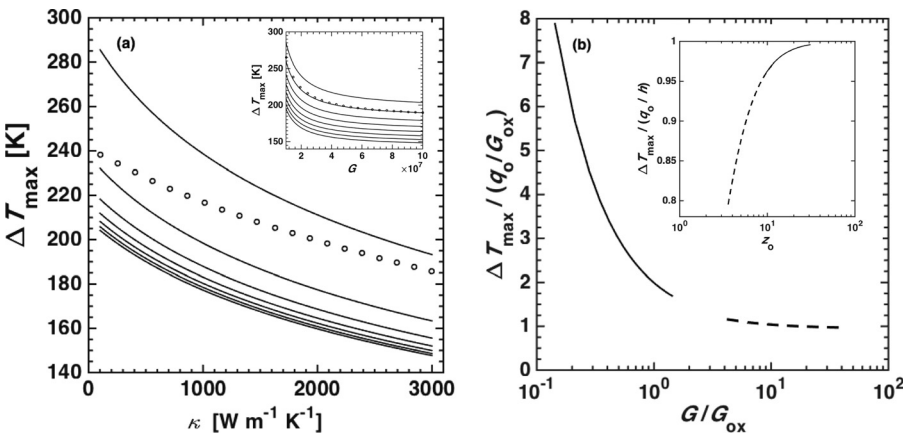

FIG. 3. (a) The calculated maximum temperature rise as a function of the basal-plane thermal conductivity κ for different interfacial conductance G values in the range between $1 \times 10^7\,W\,m^{-2}\,K^{-1}$ (top curve) and $1 \times 10^8\,W\,m^{-2}\,K^{-1}$ (bottom curve) in increments of $1.5 \times 10^7\,W\,m^{-2}\,K^{-1}$ for the case of a 300-nm-thick dielectric. The inset shows the maximum temperature rise as a function of increasing G for different κ in the range between $100\,W\,m^{-1}\,K^{-1}$ (top curve) and $2900\,W\,m^{-1}\,K^{-1}$ in $400\,W\,m^{-1}\,K^{-1}$ increments. Representative curves calculated from the analytical solution of Eq. (2) are pictured as open circles. (b) Normalized maximum temperature rise calculated by the analytical model as a function of the G/G_{ox} ratio (main figure) and the z_0 parameter (inset). The solid and dashed lines are for graphene devices made on a 10- and 300-nm-thick SiO_2 dielectric on a high thermal conductivity substrate, respectively. The graphene basal-plane thermal conductivity is kept as $600\,W\,m^{-1}\,K^{-1}$ for the main figure, and ranges between 300 and $3000\,W\,m^{-1}\,K^{-1}$ for the inset, where G is taken as $4 \times 10^7\,W\,m^{-2}\,K^{-1}$.

attained for an interface conductance of $1 \times 10^7\,\mathrm{W\,m^{-2}\,K^{-1}}$. Interestingly, increasing or decreasing G has a relatively little effect on these results. For example, for the same range of κ, but with an order of magnitude of larger interfacial conductance, a 20 K drop in ΔT_{max} is still observed.

These observed sensitivities of the hot spot maximum temperature to κ and G can be better understood with the use of the following simplified heat diffusion equation for the graphene channel in cylindrical coordinates, where the dependence on the azimuthal angle has been ignored

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{dT}{dr}\right) - \frac{h}{\kappa t}(T - T_\infty) + \frac{\dot{q}'''}{\kappa} = 0, \tag{2}$$

where r is the radial distance from the center of the hot spot, $t = 0.335$ nm is the thickness of graphene, $\dot{q}'''$ is volumetric heating in $\mathrm{W\,m^{-3}}$, and h is the vertical heat transfer coefficient between graphene and the underlying silicon heat sink and is calculated as

$$h = \left(\frac{1}{G_{ox}} + \frac{1}{G}\right)^{-1}, \tag{3}$$

where $G_{ox} = \frac{\kappa_{ox}}{t_{ox}}$ is the vertical thermal conductance per unit area of the oxide layer. The volumetric heating term represents the joule heat concentrated around the defect and is approximated as a Gaussian distribution,

$$\dot{q}''' = q_0/t \exp\left(-\frac{r^2}{r_o^2}\right), \tag{4}$$

where r_o is a characteristic width of the localized heating spot. A value for r_o of 1.75 μm was obtained from the numerical simulation according to a fit of the J^2 profile, where J is the simulated current density. The constant q_0 is obtained from the fit such that the total generated Joule heat is identical to that considered in the simulation. Equation (2) can be solved to obtain the temperature rise as a function of the non-dimensional term $z \equiv r/l$, where $l = (\kappa t/h)^{\frac{1}{2}}$ represents a heat spreading length, according to

$$\Delta T(z) = C_1 I_o(z) + C_2 K_o(z) + \Delta T_p(z). \tag{5}$$

In this solution, $\mathrm{I_o}$ and $\mathrm{K_o}$ are the zeroth-order modified Bessel functions of the first and second kind, respectively.[20] The particular solution is of the form

$$\Delta T_p(z) = I_o(z)\int_0^z \frac{K_o(z)\frac{q_0}{h}\exp\left(-\frac{z^2}{z_o^2}\right)}{-I_o(z)K_1(z) - K_o(z)I_1(z)}dz - K_o(z)\int_0^z \frac{I_o(z)\frac{q_0}{h}\exp\left(-\frac{z^2}{z_o^2}\right)}{-I_o(z)K_1(z) - K_o(z)I_1(z)}dz, \tag{6}$$

where $z_0 \equiv r_0/l$. When subjected to the boundary conditions of a vanishing gradient at $r = 0$ and $\lim_{r\to\infty} T(r) = T_\infty$, $C_1 = -\lim_{z\to\infty}(\Delta T_p(z)/I_o(z))$ and $C_2 = 0$.[20] Furthermore, the solution for the maximum temperature rise occurs at $z = 0$, where $\Delta T_p = 0$ and $I_o = 1$. As such, $\Delta T_{\max} = C_1$, which exhibits a similar dependence on G and κ as the numerical results, as shown by the open symbols in Fig. 3(a).

This analytical model shows that $\Delta T_{\max}$ decreases with decreasing $q_0(1 + \frac{G_{ox}}{G})/G_{ox}$. Increasing G from 2×10^7 $\mathrm{W\,m^{-2}\,K^{-1}}$ to $2 \times 10^8\,\mathrm{W\,m^{-2}\,K^{-1}}$ only results in a small decrease of $\Delta T_{\max}$ for the case of a 300 nm SiO_2 where $G_{ox} \approx 4.7 \times 10^6\,\mathrm{W\ m^{-2}\,K^{-1}}$. This result arises because the G/G_{ox} ratio is larger than 4, such that the thermal resistance of the 300-nm-thick oxide dominates the interface thermal resistance even for non-functionalized graphene where G can be as low as $2 \times 10^{-7}\,\mathrm{W\,m^{-2}\,K^{-1}}$.[21,22] However, when the oxide thickness is reduced to 10 nm such that G_{ox} increases to about $1.4 \times 10^8\,\mathrm{W\,m^{-2}\,K^{-1}}$, increasing G from $2 \times 10^7\,\mathrm{W\,m^{-2}\,K^{-1}}$ to $2 \times 10^8\,\mathrm{W\,m^{-2}\,K^{-1}}$ via surface functionalization[23] or other means results in an increase of the G/G_{ox} ratio from about 0.14 to 1.4. This large increase helps to reduce $\Delta T_{\max}$ by nearly one order of magnitude, provided that the electron mobility of graphene is not reduced, and is shown in Fig. 3(b).

In addition, the analytical model shows that $\Delta T_{\max}$ decreases with a decrease in $z_0 = r_0/l$. When κ is increased from $300\,\mathrm{W\,m^{-1}\,K^{-1}}$ to $3000\,\mathrm{W\,m^{-1}\,K^{-1}}$ for the 300 nm thick SiO_2 device with a G value of about $4 \times 10^7\,\mathrm{W\,m^{-2}\,K^{-1}}$,[21,22] the heat spreading length $l = (\kappa t/h)^{\frac{1}{2}}$ increases from 155 nm to 490 nm causing z_0 to decrease from 11 to 3.6. This increased l value is still smaller than the 6 μm lateral size of the graphene channel, so that the heat generated at the defect is not effectively spread to the metal electrodes. However, the l value becomes appreciable relative to the localized heat generation spot size r_0 of 1750 nm. The hot spot is therefore spread to a larger dimension laterally than r_0. Consequently, the effective area for vertical heat transfer from the hot spot through the oxide to the Si heat sink is increased, reducing $\Delta T_{\max}$ for the same localized heating profile. This trend is shown in the inset of Fig. 3(b). In contrast, when the oxide thickness is reduced to 10 nm, the heat spreading length is reduced to 57 nm and 179 nm for κ values of 300 to $3000\,\mathrm{W\,m^{-1}\,K^{-1}}$, respectively. This length range is about one order of magnitude smaller than r_0 and corresponds to z_0 in the range between 30 and 9.8. As such, the relative increase in the hot spot area due to heat spreading is small. Increasing κ is therefore relatively ineffective for reducing $\Delta T_{\max}$ for the thin dielectric case, as illustrated in the inset of Fig. 3(b).

These SThM and EFM measurement results have revealed localized hot spots around a defect introduced in the transfer process of a CVD grown graphene channel onto a SiO_2/Si substrate. The numerical electro-thermal model is able to explain the measurement results based on reported thermal conductivity and thermal interface conductance values of supported graphene. The analytical model further clarifies that increasing the thermal interface conductance G from the level of $4 \times 10^7\,\mathrm{W\,m^{-2}\,K^{-1}}$, as measured for non-functionalized graphene, is effective in reducing the hot spot temperature for devices made with a sub-10 nm gate dielectric on a high thermal conductivity substrate. However, when the cross-plane thermal conductance G_{ox} of the gate dielectric is less than about $5G$, as is the case for devices made with a relatively thick gate dielectric or on a low-thermal conductivity polymeric substrate, increasing G

via surface functionalization of graphene is ineffective. Furthermore, such functionalization can be counterproductive if the basal-plane thermal conductivity is reduced as a consequence of the functionalization process. In comparison, for a graphene device made on a 300 nm SiO_2 dielectric layer, increasing the graphene basal plane thermal conductivity from 300 $W\,m^{-1}\,K^{-1}$ toward 3000 $W\,m^{-1}\,K^{-1}$ can considerably increase the heat spreading length l compared to a micron-scale localized heat generation spot size, r_0, around a defect. This effect acts to increase the area for vertical heat transfer through the gate dielectric thereby reducing the peak temperature. This mechanism is effective even when lateral heat spreading from the hot spot to the metal electrodes is inefficient, i.e., when the lateral size of the graphene channel is much larger than l. However, the effect of increasing thermal conductivity becomes ineffective when l becomes considerably smaller than r_0, such as in a device made with a sub-10 nm gate dielectric on a high-thermal conductivity substrate. These results suggest that the hot spot temperature is sensitive to varying G and κ when the G/G_{ox} ratio and the r_0/l ratio are below about 5, respectively.

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[1]K. Novoselov, A. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, V. Grigorieva, and A. Firsov, Science **306**, 666 (2004).
[2]S. Z. Butler, S. M. Hollen, L. Cao, Y. Cui, J. A. Gupta, H. R. Gutiérrez, T. F. Heinz, S. S. Hong, J. Huang, A. F. Ismach, E. Johnston-Halperin, M. Kuno, V. V. Plashnitsa, R. D. Robinson, R. S. Ruoff, S. Salahuddin, J. Shan, L. Shi, M. G. Spencer, M. Terrones, W. Windl, and J. E. Goldberger, ACS Nano **7**, 2898 (2013).
[3]A. C. Ferrari, F. Bonaccorso, V. Fal'ko, K. S. Novoselov *et al.*, Nanoscale **7**, 4598 (2015).
[4]D. Akinwande, N. Petrone, and J. Hone, Nat. Commun. **5**, 5678 (2014).
[5]A. Shakouri, Proc. IEEE **94**, 1613 (2006).
[6]D. G. Cahill, P. V. Braun, G. Chen, D. R. Clarke, S. Fan, K. E. Goodson, P. Keblinski, W. P. King, G. D. Mahan, A. Majumdar, H. J. Maris, S. R. Phillpot, E. Pop, and L. Shi, Appl. Phys. Rev. **1**, 011305 (2014).
[7]A. L. Moore and L. Shi, Mater. Today **17**, 163 (2014).
[8]M. M. Sadeghi, S. Park, Y. Huang, D. Akinwande, Z. Yao, J. Murthy, and L. Shi, J. Appl. Phys. **119**, 235101 (2016).
[9]J. Kang, D. Shin, S. Bae, and B. H. Hong, Nanoscale **4**, 5527 (2012).
[10]C. J. An, S. J. Kim, H. O. Choi, D. W. Kim, S. W. Jang, M. L. Jin, J.-M. Park, J. K. Choi, and H.-T. Jung, J. Mater. Chem. A **2**, 20474 (2014).
[11]J. Choi, H. Kim, J. Park, M. W. Iqbal, M. Z. Iqbal, J. Eom, and J. Jung, Curr. Appl. Phys. **14**, 1045 (2014).
[12]H. H. Kim, S. K. Lee, S. G. Lee, E. Lee, and K. Cho, Adv. Funct. Mater. **26**, 2070 (2016).
[13]Z. Yan, G. Liu, J. M. Khan, and A. A. Balandin, Nat. Commun. **3**, 827 (2012).
[14]Z. Gao, Y. Zhang, Y. Fu, M. Yuen, and J. Liu, Carbon **61**, 342 (2013).
[15]E. Pop, V. Varshney, and A. Roy, MRS Bull. **37**, 1273 (2012).
[16]L. Shi, O. Kwon, A. C. Miner, and A. Majumdar, J. Microelectromech. Syst. **10**, 370 (2001).
[17]K. Kim, J. Chung, J. Won, O. Kwon, J. S. Lee, S. H. Park, and Y. K. Choi, Appl. Phys. Lett. **93**, 203115 (2008).
[18]K. Kim, J. Chung, G. Hwang, O. Kwon, and J. S. Lee, ACS Nano **5**, 8700 (2011).
[19]I. Jo, I. K. Hsu, Y. J. Lee, M. M. Sadeghi, S. Kim, S. Cronin, E. Tutuc, S. K. Banerjee, Z. Yao, and L. Shi, Nano Lett. **11**, 85 (2011).
[20]W. Cai, A. L. Moore, Y. Zhu, X. Li, S. Chen, L. Shi, and R. S. Ruoff, Nano Lett. **10**, 1645 (2010).
[21]Y. K. Koh, M. Bae, D. G. Cahill, and E. Pop, Nano Lett. **10**, 4363 (2010).
[22]K. F. Mak, C. H. Lui, and T. F. Heinz, Appl. Phys. Lett. **97**, 221904 (2010).
[23]P. E. Hopkins, M. Baraket, E. V. Barnat, T. E. Beechem, S. P. Kearney, J. C. Duda, J. T. Robinson, and S. G. Walton, Nano Lett. **12**, 590 (2012).