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APPLIED PHYSICS LETTERS VOLUME 84, NUMBER 11 15 MARCH 2004

Multilevel memory based on molecular devices

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(Received 8 October 2003; accepted 14 January 2004)

Multilevel molecular memory devices were proposed and demonstrated for nonvolatile data storage up to three bits (eight levels) per cell, in contrast to the standard one-bit-per-cell (two levels) technology. In the demonstration, charges were precisely placed at up to eight discrete levels in redox active molecules self-assembled on single-crystal semiconducting nanowire field-effect transistors. Gate voltage pulses and current sensing were used for writing and reading operations, respectively. Charge storage stability was tested up to retention of 600 h, as compared to the longest retention of a few hours previously reported for one-bit-per-cell molecular memories. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1667615]

The past fifty years has witnessed continuous memory density increases and lower cost per bit, which has been powered by the startling downscaling of silicon memory devices. This trend, however, may soon end due to physical and technical limitations. Continued growth of the semiconductor industry will likely rely on breakthroughs in both electronic materials and also device concepts. Extensive efforts have been devoted to address these two issues, and molecular memory is considered particularly promising. Such a memory has the potential to work on a few electrons at molecular scale and therefore promises low-power and ultradense systems. Recent advances have been made for standard one-bit-per-cell molecular memory demonstration with retention time ranging from seconds to a few hours.[1–4] This work reports on multilevel molecular memory devices for up to three bits per cell with retention up to 600 h.

Storage of multiple bits on a single memory cell multiplies the density in the same space and has received increasingly more attention from the semiconductor industry. These devices rely on hot electron injection from the channel into the floating gate through a tunneling oxide layer, and different memory states are represented by different amount of charges stored, as shown in Fig. 1. Further decreasing the cell size or increasing the number of levels for higher density, however, is extremely difficult, as the complicated device structure and the topdown fabrication approach inevitably leads to significant device variation and a blurring of the multiple levels.[5] Molecular electronics may offer a solution to this scaling limit by taking advantage of the bottom-up self-assembling process. On one hand, discrete multilevels naturally exist in an ensemble of redox-active molecules,[6] or even one molecule containing multiple redox centers.[7] On the other hand, precise charge sensing at discrete levels can be carried out with a semiconducting nanowire transistor[8,9] whose conductance is ultrasensitive to charges in the surrounding environment. Thus, a multilevel memory can be made, for example, from redox molecules interfaced with a nanowire, as shown in Fig. 1. The data storage can be carried out by altering the population of the reduced/oxidized molecules, while the readout can be implemented by measuring the conduction of the nanowire. A two-level memory has been demonstrated before with excellent performance.[3]

For this study we used field effect transistors based on 10 nm In_2O_3 nanowire synthesized via laser ablation (Fig. 2).[8,9] Functionalization of the nanowire surface was carried out by immersing the as-fabricated devices into a 0.5 mM solution of the desired molecular wires, which can be absorbed onto the In_2O_3 surface.[10] In_2O_3 film test samples were prepared according to a previously reported method.[11]

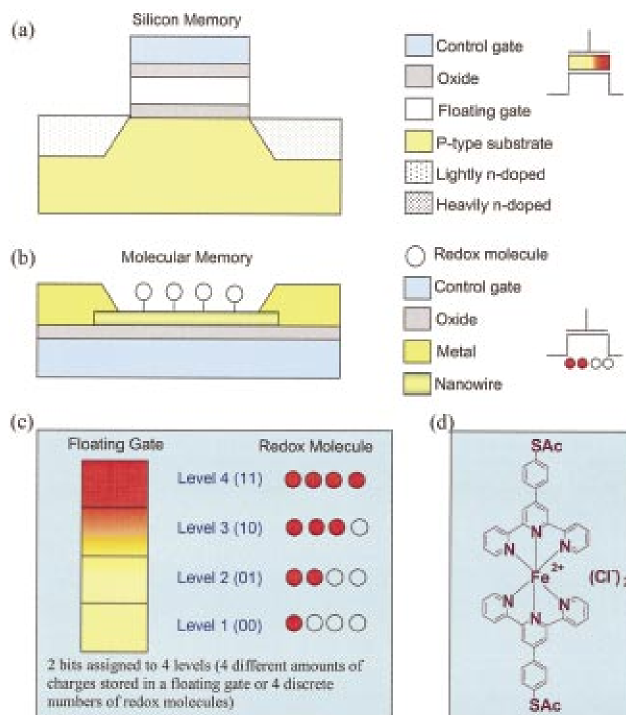

FIG. 1. (Color) Schematic diagram compares silicon flash memory (a) and the proposed molecular memory (b) for multilevel nonvolatile data storage. (c) In a 2-bit silicon memory cell, four different amounts of charges are placed in the floating gate via channel hot electron injection. In contrast, multilevels in our memory cells are represented by altering the population of the reduced/oxidized molecules by applying gate voltage pulses of different amplitude; (d) illustrated molecule is a Fe^{2+}-terpyridine compound used in this study.

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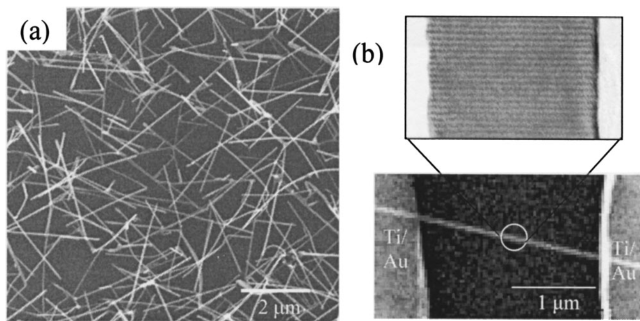

FIG. 2. (a) SEM micrograph of single-crystalline In_2O_3 nanowires synthesized via a laser ablation approach; (b) SEM micrograph of an In_2O_3 nanowire transistor. Inset: a high-resolution TEM image of an In_2O_3 nanowire.

Ellipsometry was performed over such samples before and after the molecule deposition, and a monolayers thickness ~ 20 Å was detected. Our memory utilizes an active area of 2 μm (channel length) by 10 nm (nanowire width), indicating a storage density of 40 Gbits/cm^2 by assuming each cell can be programmed into eight levels. More importantly, our devices boast much simplified fabrication process and device structure compared to silicon flash memory, as only one step of photolithography and metallization are required for our approach, whereas multiple fabrication steps are required for silicon flash memory. As a result, our memory structure has great potential for ultradense data storage by further decreasing the cell size to nanoscale or increasing the number of levels.

Figures 3 and 4 illustrate characteristic multilevel data storage for a device containing Fe-terpyridine redox molecules. All our measurements were performed at room temperature with the device residing in a high vacuum chamber to eliminate the effect of moisture. Figure 3(a) shows a family of $I-V_g$ hysteresis loops taken with different lower- and higher-bound values for the V_g sweep. From the innermost $I-V_g$ loop to the outmost one, the corresponding lower-bound and higher-bound values are $(-n*2.5\ \mathrm{V},\ 10+n*2.5\ \mathrm{V})$ in which n is the index of levels from 1 to 8 (the curve corresponding to $n=1$ omitted for clarity). One can clearly see that different negative gate biases can bring the device to different conduction levels at $V_g=0$ V. Programming of the memory device can therefore be achieved by sweeping V_g from 0 to different negative values, or by applying negative V_g pulses of different amplitude. On the other hand, erasing of the memory device can be easily achieved by sweeping V_g from 0 to a large positive value (e.g., 25 V), or by applying a V_g pulse of 25 V, which leaves the device in a highly resistive state. This is also evident in Fig. 3(b), where a family of $I-V$ curves were taken at $V_g=0$ V after the device was written into various memory levels (denoted state "0" to "8") using V_g pulses of different amplitude. These curves represent distinctively different conduction levels, thus indicating the effectiveness of the memory programming and the feasibility of using current sensing to read out the memory state. Control experiments have been done with bare nanowire transistors without self-assembled molecules, and little hysteresis was observed, indicating the importance of the redox molecules for the above-mentioned memory effect. The different states of our memory devices are attributed to different populations of the oxidized molecular wires, as a higher negative gate bias is expected to bring more negative charges to the Si/SiO_2 interface and correspondingly more positive charges to the nanowire/molecules, thus leaving more molecules in the oxidized state.

Our writing paradigm represents a significant departure from the channel hot electron (CHE) injection commonly used for silicon flash memory, where a high driving field (in the order of 10 V/μm) is applied to the source–drain channel for hot electron charge injection.[5] Such high source–drain biases lead to significant power consumption and the formation of interface traps, thus making the long-term operation error prone. In contrast, our devices can be programmed into multiple levels by applying gate biases of different amplitude with 0 V applied to the source and drain, and the readout is usually carried out with a small electric field ~ 0.05 V/μm

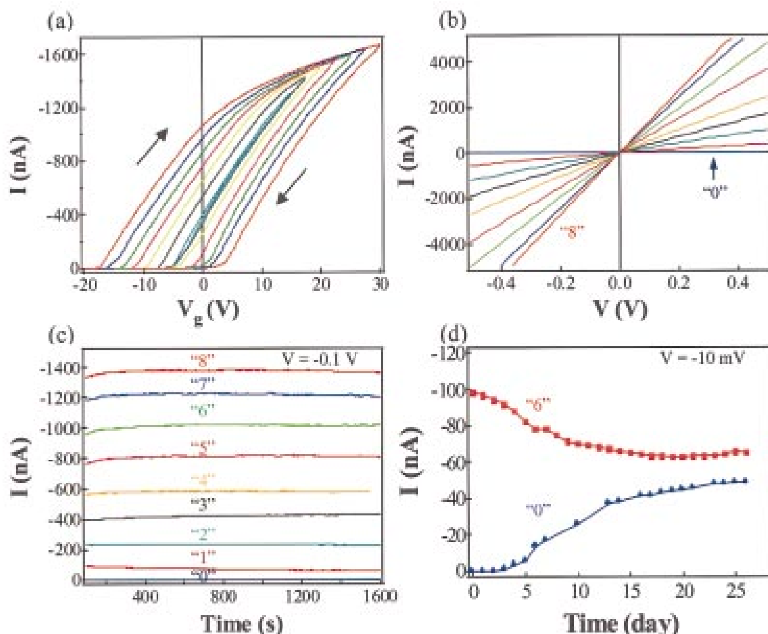

FIG. 3. (Color) Characteristic programming and erasing (charge placement), reading (current sensing) and retention (charge storage stability) obtained from the proposed devices containing Fe^{2+}-terpyridine molecules: (a) $I-V_g$ hysteresis loops obtained by sweeping gate voltage from $-n*2.5$ V to $10+n*2.5$ V and then back to the starting value. n is the index of levels from "2" (the innermost curve) to "8" (the outermost curve). (b) $I-V$ characteristics recorded after the device was written using V_g pulses of $+25$, -2.5, -5, -7.5, -10, -12.5, -15, -17.5, and -20 V, respectively, from the least conductive curve to the most conductive one; (c) current recorded over time after the device was written into states "0" (the bottom curve) to "8" (the top curve). Little degradation in the stored signal was observed over 1500 s with a source-drain bias of $V=-0.1$ V; (d) extended retention measurements performed for state "0" and "6" with a source-drain bias of $V=-10$ mV.

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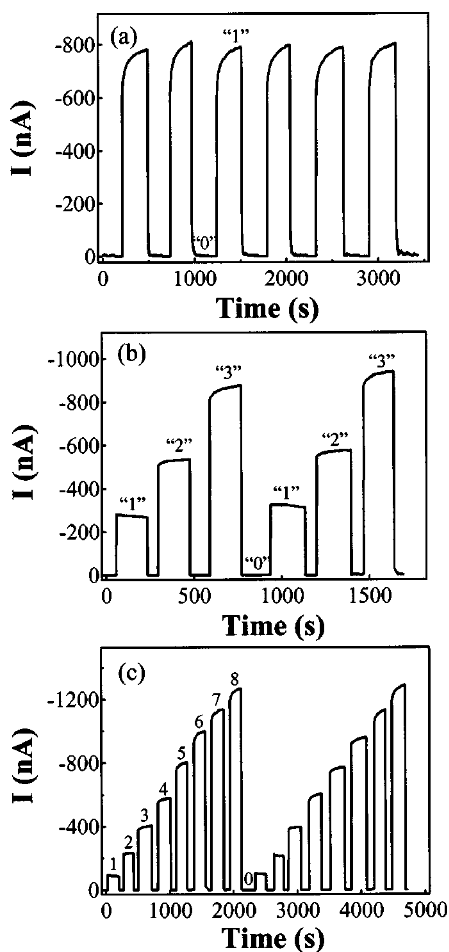

FIG. 4. Endurance test characterized by cycling of write-erase-read operations for 1, 2, and 3 bits data storage at 2(a), 4(b), and 8(c) levels, respectively.

applied to the nanowire channel. Obviously, the required power for operation is much less than that for silicon flash memory.

The retention of our memory devices was characterized for nonvolatile applications. Figure 3(c) shows the retention time measurements taken with fixed source-drain bias $V=-0.1$ V for memory states "0"–"8" right after the writing was performed. All the states showed little degradation over time and remain clearly separated from each other even after 1500 s. Furthermore, no matter what initial states the device stays at, a positive voltage pulse of 25 V can always write the device into the off state (state "0"), which remains nonconductive for a long period of time, as shown in the bottom curve in Fig. 3(c). The on/off ratio between state "0" and state "8" is estimated to be 10^4 throughout this duration. Extended stability test was carried out up to retention of 600 h. The readout current at each of the eight levels remained within 80% variation for the first 120 h (five days). Figure 3(d) shows extended retention test results for state "0" and state "6" measured with a source–drain bias $V=-10$ mV. Both states were very stable and exhibited slow decays over a period of many days. They eventually reached steady states, featured by current values of 63 nA from initial 100 nA for state "6" and 48 nA from initial 10^{-2} nA for state "0." These levels are still distinguishable since the white noise is on the order of ~ 1 nA. The molecular memory illustrated in this work promises greatly enhanced retention or charge storage ability at nano/molecular scale through appropriate molecular design, thus offers an attractive solution to problems resulting from poor charge storage in downscaling of current silicon flash memory.[12]

We have further carried out writing/reading/erasing operations in real time domain for storage of 1, 2, and 3 bits in the same cell, respectively, at two, four, and eight levels, as shown in Fig. 4. For one-bit (two-level) memory, the device was repeatedly written into state "0" and "1" by applying alternating V_g pulses of 25 and -12.5 V. The memory state after each writing operation was read out at $V_g=0$ V with a source–drain voltage of -0.1 V, and the data are plotted in Fig. 4(a). For two-bit operation, the memory cell was written into state "0," "1," "2," and "3" using V_g pulses of 25, -5, -10, and -15 V, respectively, as shown in Fig. 4(b). V_g pulses of 25 V were also used to erase the previous memory state for the ensued writing. Three-bit memory operations were similarly carried out using V_g pulses of $+25$, -2.5, -5, -7.5, -10, -12.5, -15, -17.5, and -20 V, and the data are shown in Fig. 4(c). We repeated tens of cycles for endurance test for each memory operation and found that all levels were distinguishable in the tested cycles.

In summary, we have demonstrated multilevel nanoscale memory devices based on nanowire field effect transistors with self-assembled redox active molecules. By creating a seamless integration of nanowires and molecular wires, our multilevel data storage represents a conceptual breakthrough in molecular memory and yielded devices with on/off ratios exceeding 10^4 and retention times ~ 600 h.

The authors thank USC, NSF CAREER Program, NASA Contract No. NAS2-99092, NSF CENS Program, and a SRC/MARCO Grant for financial assistance, and Dr. Bin Yu, Dr. Houte Ng, Dr. Jun Li, Dr. Harry Patridge for discussion. W.F., S.A., and J.H. are employees by Eloret Corporation during this work which was supported by a NASA contract to Eloret.

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