High-Performance Single-Crystalline Arsenic-Doped Indium Oxide Nanowires for Transparent Thin-Film Transistors and Active Matrix Organic Light-Emitting Diode Displays

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ABSTRACT We report high-performance arsenic (As)-doped indium oxide (In$_2$O$_3$) nanowires for transparent electronics, including their implementation in transparent thin-film transistors (TTFTs) and transparent active-matrix organic light-emitting diode (AMOLED) displays. The As-doped In$_2$O$_3$ nanowires were synthesized using a laser ablation process and then fabricated into TTFTs with indium—tin oxide (ITO) as the source, drain, and gate electrodes. The nanowire TTFTs on glass substrates exhibit very high device mobilities ($\sim 1490$ cm$^2$ V$^{-1}$ s$^{-1}$), current on/off ratios ($5.7 \times 10^5$), steep subthreshold slopes (88 mV/dec), and a saturation current of 60 $\mu$A for a single nanowire. By using a self-assembled nanodielectric (SAND) as the gate dielectric, the device mobilities and saturation current can be further improved up to 2560 cm$^2$ V$^{-1}$ s$^{-1}$ and 160 $\mu$A, respectively. All devices exhibit good optical transparency ($\sim 81\%$ on average) in the visible spectral range. In addition, the nanowire TTFTs were utilized to control green OLEDs with varied intensities. Furthermore, a fully integrated seven-segment AMOLED display was fabricated with a good transparency of $40\%$ and with each pixel controlled by two nanowire transistors. This work demonstrates that the performance enhancement possible by combining nanowire doping and self-assembled nanodielectrics enables silicon-free electronic circuitry for low power consumption, optically transparent, high-frequency devices assembled near room temperature.

KEYWORDS: transparent electronics · metal oxide nanowire synthesis · self-assembled gate dielectric (SAND) · AMOLED display

Recently, one-dimensional (1-D) nanostructured materials, including single-walled carbon nanotubes (SWNTs) and semiconductor metal oxide nanowires, have been considered as another material choice for TTFT fabrications. In comparison to conventional TCO-based TTFTs, nanomaterials synthesized through a simple chemical vapor deposition (CVD) method can easily provide high-quality single-crystalline nanostructures, which are highly desirable in most electronic and optoelectronic devices. In addition, nanostructured material-based TTFTs have added advantages, such as versatile...
compatibility with a variety of device substrates, which thereby extends their applicability to flexible electronics, due to the compatibility of nanostructured TFTs with low-temperature processing. Among these nanomaterials, the In$_2$O$_3$ nanowire having a wide energy gap (~3.75 eV), a single-crystalline nanostructure, and high device mobility is one of the best candidates for high-performance TFTs.

Our research group and Ju et al. have also demonstrated In$_2$O$_3$ nanowire TFTs with a device mobility as high as 514 cm$^2$ V$^{-1}$ s$^{-1}$. However, this performance is still low compared to nontransparent devices,

In considering the enablers of next-generation displays, having good optical transparency and/or mechanical flexibility, high-performance transparent and/or flexible TFTs will be essential. For example, the circuitry of an AMOLED pixel usually contains one driving transistor and one switching transistor. The driving transistors must carry sufficient current to the OLED pixels, and the switching transistors must be able to operate at 60–120 Hz for the human eye to see an integrated image of successively presented patterns in a video display (so-called retinal persistence). Currently, polycrystalline silicon (poly-Si) and amorphous silicon (a-Si) are widely used as the “back-panel” electronics for AMOLED displays. However, these back-panels are usually optically opaque, not compatible with flexible substrates, and have drawbacks such as low mobilities, high threshold voltages, and, in the case of a-Si, poor current-carrying capacity.

In this contribution, we first report the synthesis of arsenic (As)-doped In$_2$O$_3$ nanowires on Si/SiO$_2$ substrates and then fabricate TFTs by transferring the doped nanowires to glass substrates with prepatterned indium–tin oxide (ITO) gate electrodes and an Al$_2$O$_3$ or a self-assembled nanodielectric (SAND) gate insulator, followed by patterning transparent ITO source and drain electrodes. It will be seen that the as-fabricated As-doped In$_2$O$_3$ nanowire TFTs perform as typical n-type FETs with a high device mobility (1490 cm$^2$ V$^{-1}$ s$^{-1}$) and optical transparency of near 81% in the visible wavelength regime. We further examine the AC gain of these nanowire TFTs, to the best of our knowledge, the first AC gain study of nanowire TFTs. The results indicate good frequency response, ~1.5 kHz with a unity-gain frequency of ~18.8 GHz. Moreover, we then show that As-doped In$_2$O$_3$ nanowire TFTs can be used to drive organic light-emitting diodes (OLEDs) with tunable emitting intensities, including a seven-segment AMOLED display enabled by a nanowire TFT “back-panel”.

**RESULTS AND DISCUSSION**

Characterization of Arsenic-Doped Indium Oxide Nanowires. As-doped In$_2$O$_3$ nanowires used in this study were grown on a Si/SiO$_2$ substrate by a laser ablation process. In contrast to our previous work using argon mixed with oxygen as the carrier gas, we intentionally added hydrogen to the carrying gas to suppress the oxidation processes and incorporate a small amount of As into the In$_2$O$_3$ nanowires. The surface morphology and crystal structure of the As-doped In$_2$O$_3$ nanowires was further characterized by field-emission scanning electron microscopy (FESEM), high-resolution transmission electron microscopy (HRTEM), selected area electron diffraction pattern (SAED), and energy dispersion X-ray spectrometry (EDS). Figure 1a shows a typical SEM image of as-grown As-doped In$_2$O$_3$ nanowires which are ~5–10 μm long with a diameter of 15–30 nm. A Au/In alloy particle, with a diameter of ~16 nm, can be clearly observed at the very tip of the nanowire, supporting growth via a so-called vapor–liquid–solid (VLS) growth mechanism (Figure 1a, inset). In addition, the As-doped In$_2$O$_3$ nanowires have perfectly smooth surfaces without any amorphous coating and have extremely uniform diameters. To further evaluate the composition of the As-doped In$_2$O$_3$ nanowires, EDS was performed during the TEM investigation. Figure 1b shows a typical EDS spectrum of an individual As-doped In$_2$O$_3$ nanowire, which indicates the presence of As elements in In$_2$O$_3$ nanowires. The atomic ratio of In/As is estimated to be 100:4. The atomic density of In$_2$O$_3$ is about 3.12 × 10$^{22}$ atom/cm$^3$, and the dopant density of 4% As dopants can be estimated to be 1.25 × 10$^{21}$ atom/cm$^3$. However, the actual amount of As atoms incorporated into the crystal sites of In$_2$O$_3$ nanowires is not clear and required more detailed experiments.

The crystallography of these As-doped nanowires was also studied using HRTEM and SAED. HRTEM confirms that each As-doped In$_2$O$_3$ nanowire has a perfect single-crystalline structure without any noticeable dislocations or defects, and the corresponding SAED reveals that the phase of As-doped nanowires is body-centered cubic (bcc), as shown in Figure 1c. The interspacing between each plane is 0.506 nm, corresponding to the (200) plane in the bcc As-doped In$_2$O$_3$ nanowire crystal structure (shown in Figure 1d), with the lattice constant (a) of 1.012 nm slightly expanded versus that of undoped In$_2$O$_3$ nanowires (a = 1.01 nm). The expanded lattice constant can be attributed to the incorporation of As into the In$_2$O$_3$ nanowires. Taken together, these results indicate that these nanowires grown using the present laser ablation process exhibit high crystalline quality, with the In$_2$O$_3$ nanowire structural integrity preserved after As dopant incorporation.
Electronic Transport Characteristics of As-Doped In$_2$O$_3$ Nanowire TFTs. It is well-known that doping processes can substantially enhance the electrical properties of nanowire materials in a controlled fashion, and that zinc, antimony, and arsenic are all effective n-type dopants which increase the carrier concentration in In$_2$O$_3$ thin films. Here we focus on As-doped In$_2$O$_3$ nanowires as the semiconductor in TFT devices. After the nanowire synthesis, the as-grown nanowires were removed from the Si/SiO$_2$ substrates by ultrasonication to yield a suspension in isopropyl alcohol (IPA) and were then dispersed onto an ITO substrate with 50 nm Al$_2$O$_3$ dielectric. The process was performed repeatedly until the desired nanowire density was achieved, and then ITO was deposited as source and drain electrodes. The nanowire orientation is random, but with desired density, we can achieve a yield of 80% for the transistors. Figure 2a shows a schematic of an As-doped In$_2$O$_3$ nanowire TFT on an ITO glass substrate, with an atomic layer deposition (ALD)-derived high-$k$ Al$_2$O$_3$ (thickness of 50 nm, $k_{eff} \sim 9.0$) dielectric layer, and ion-assisted deposition-derived (IAD) ITO (thickness of 100 nm, sheet resistance $\sim 60 \ \Omega/\square$) source and drain electrodes, with the semiconductor-doped metal oxide nanowires as the active channel. Details can be found in the Supporting Information. Figure 2b displays the optical image of an As-doped In$_2$O$_3$ nanowire TFT substrate, with the background photograph visible through the transistor regions. The transmittance spectrum in the Supporting Information (Figure S3) reveals $\sim 81\%$ optical transmission, essentially identical to that of bare glass or glass/ITO substrates.

Detailed electronic transport measurements were carried out to characterize the electronic properties of single As-doped In$_2$O$_3$ nanowire TFTs. The measured drain current ($I_{ds}$) versus source–drain voltage ($V_{DS}$) characteristics of a representative single nanowire TFT is shown in Figure 2c. The channel length of the as-fabricated TFTs is $\sim 1.8 \ \mu$m, shown in the inset SEM image of Figure 2d (scale bar = 1 \ \mu m). The device exhibits typical enhancement-mode n-type semiconductor transistor behavior with an on-current ($I_{on}$) of $\sim 60 \ \mu A$, while $V_{g} = 4.5 \ \text{V}$ and $V_{DS} = 3 \ \text{V}$. Note that doping helps to reduce the contact resistance in In$_2$O$_3$ nanowire FETs, shown by the absence of a Schottky barrier in Figure 2c.

Figure 2d shows the drain current ($I_{ds}$) versus gate voltage ($V_{g}$) characteristics for a single transparent As-doped In$_2$O$_3$ nanowire transistor. The doped In$_2$O$_3$ nanowire devices display $I_{on}/I_{off} = 5.7 \times 10^6$, a peak sub-threshold slope ($S$) = 88 mV/dec, and threshold voltage ($V_T$) = 0.5 V, while $V_{DS} = 200 \ \text{mV}$. The mobility ($\mu$) was calculated from the maximum transconductance by applying the eqs 1 and 2.

$$\mu = \frac{I_d^2}{V_{DS}C_{ox}} \times \frac{dI_{DS}}{dV_g} \quad (1)$$
Figure 2. Fabrication of fully transparent As-doped In$_2$O$_3$ nanowire transistors. (a) Schematic diagram of As-doped In$_2$O$_3$ nanowire TFT fabricated on an ITO glass substrate, with ALD-deposited Al$_2$O$_3$ or SAND as the dielectric layer and IAD-deposited ITO as source and drain electrodes. (b) Optical photograph of fully transparent As-doped In$_2$O$_3$ nanowire transistors. The substrate area is marked with a yellow frame for clarity. (c) Family of $I_{ds}$ versus $V_g$ curves of a single As-doped In$_2$O$_3$ nanowire TFT with the channel length of 1.8 $\mu$m. The gate voltage varied from $-4.5$ to $4.5$ V in a step of $1.5$ V from bottom to top. Inset: SEM image of an As-doped In$_2$O$_3$ nanowire bridging ITO electrodes. (d) Current versus gate voltage ($I_{ds}$ versus $V_g$) plot in the linear regime ($V_{DS} = 200$ mV). Red, green, and blue curve correspond to linear-scale $I_{ds}$ versus $V_g$ and log scale $I_{ds}$ versus $V_g$, respectively. Inset shows an SEM image of the nanowire transistor. (e) Measurement setup showing As-doped In$_2$O$_3$ nanowire transistor configured as a common-source amplifier. (f) Frequency response of AC gain of As-doped In$_2$O$_3$ nanowire TFT. Solid blue line shows the measured frequency response of As-doped In$_2$O$_3$ nanowire TFT; dashed red line represents the simulated data of As-doped In$_2$O$_3$ nanowire TFT. The green solid line shows simulation data for an optimized As-doped In$_2$O$_3$ nanowire TFT. (g) Bilateral small-signal model used in this study.

where $L$ is the channel length and $C_i$ is the specific capacitance of single doped nanowire calculated as follows$^{26}$

$$C_i = \frac{2 \pi \varepsilon_i \varepsilon_0 L}{\ln(2h/r)} \quad (2)$$

where, $r$ is the radius of doped In$_2$O$_3$ nanowires, $h$ is the thickness of the dielectric layer, and $\varepsilon_i$ is the dielectric constant of ALD-deposited Al$_2$O$_3$. It is found that the device mobility varies from $\sim$1080 to 1490 cm$^2$ V$^{-1}$ s$^{-1}$ as the gate bias is increased from 1.0 to 3.0 V. In comparisons to other nanowire TFTs, the present mobilities are substantially greater, with ZnO = 20 cm$^2$ V$^{-1}$ s$^{-1}$, In$_2$O$_3$ = 35 cm$^2$ V$^{-1}$ s$^{-1}$, and SnO$_2$ = 15 cm$^2$ V$^{-1}$ s$^{-1}$.$^{1,11}$ This can be understood from the single-crystal nature of the As-doped In$_2$O$_3$ nanowires and the formation of relatively high-quality interfaces. Note that the present device performance rivals or exceeds that of previously reported doped and undoped metal oxide nanowire TFTs.$^{20,21,33,34}$

Table 1 summarizes the relevant data which suggest that the As doping should significantly enhance overall nanowire device performance. Detailed statistical study of 10 single nanowire TFTs (Figure S2, Supporting Information) reveals that the device mobility is 1200 cm$^2$ V$^{-1}$ s$^{-1}$ on average with a standard deviation of 210 cm$^2$ V$^{-1}$ s$^{-1}$, the subthreshold voltage is 170 mV/dec with a standard deviation of 90 mV/dec, and the $I_{off}/I_{on}$ ratio is from 10$^4$ to 10$^5$.

To further modify device performance, the 50 nm Al$_2$O$_3$ gate dielectric was replaced with an organic self-assembled nanodielectric (SAND), layer (thickness $\sim$16 nm, $k_{eff} \sim 5$; see the Supporting Information for details).$^{35}$ The mobility of a single As-doped In$_2$O$_3$ nanowire TFT is enhanced to $\sim$2560 cm$^2$ V$^{-1}$ s$^{-1}$ for $V_g$ and $V_{DS} = 4.4$ and 200 mV, respectively. In addition, $I_{ON}$ is increased to 160 $\mu$A at $V_g = 3.0$ V and $V_{DS} = 1.5$ V, and $S$ increased to 149 mV/dec (Figure S1a,b in the Supporting Information). These SAND effects can be attributed to the advantageous characteristics of the high-capacitance dipolar organic nanoscopic dielectrics.$^{36,37}$

A similar $I_{off}/I_{on}$ ratio ($\sim 10^9$) was previously reported for ZnO/SAND nanowire TFTs$^{38}$ and may result from the gate leakage current. The gate leakage current was measured between the source/drain pads and the back gate electrode (with overlapping area of $\sim 2 \times 10^{5}$ $\mu$m$^2$) to be about 1 nA for the 16 nm SAND dielectric and 20 pA for
the 50 nm Al₂O₃ dielectric at V_{dd} = 3 V. This gate leakage current for SAND dielectric sets a lower limit for the off current that can be reliably measured and is likely a reason for the observed I_{on}/I_{off} ratio of 10⁴ for the SAND-gated devices. We note that much of the measured leakage current may be conduction between the source/drain pads and the back gate electrode underneath, and thus the leakage current could be greatly reduced by using a patterned gate electrode with minimized overlap with the source and drain electrodes. Means to suppress this are under further investigation.

The present devices exhibit high mobilities and steep subthreshold slopes, which are desired properties for fast device operation, such as switching transistors in AMOLED displays. The unity-gain frequency of the nanowire TTFTs was estimated using eq 3, where \( V_g - V_T \) is the gate overvoltage (the applied gate voltage in excess of the threshold voltage).\(^{(3)}\)

\[
f_T = \frac{\mu(V_g - V_T)}{2nL^2}
\]

In this approximation, the unity-gain frequency of our TTFTs can reach 18.8 GHz. In addition, we also investigated the AC gain and radio frequency response (RFR) from the As-doped In₂O₃ nanowire TTFTs. Figure 2e shows the experimental setup for AC measurements. The nanowire TTFT is configured as common-source amplifier, and DC offsets are applied to the gate and drain electrodes to bias it in saturation, near the maximum \( g_{m} \) (\( \sim 1.8 \) μS). Figure 2f shows the RFR of the device measured by applying digital signal processing (DSP) to the time domain signals (blue line), simulated data for the as-fabricated TTFT (red line), and simulated data for an optimized device structure (green line). A gain of \( \sim -6 \) dB can be observed at low frequency with a roll-off around 500 Hz and a cutoff frequency \( (f_{-3\text{db}}) \) of \( \sim 1.5 \) kHz, which is comparable to earlier work. To understand the frequency response of our As-doped In₂O₃ nanowire TTFTs, a bilateral small-signal model\(^{(30)}\) (shown in Figure 2g) is applied to model the AC characteristics of the present TTFTs. The simulated result (red line) agrees well with the measured data, suggesting that the operation frequency is strongly influenced by the parasitic capacitance associated with the source and drain contact electrodes (\( \sim 157 \) pF) and the probes (\( \sim 100 \) pF). By optimizing the device dimensions and structure (i.e., use short channel widths and reduce overlaps between source and drain contact electrodes) and adopting an active probe (\( \sim 1 \) MΩ) for the measurements, the cutoff frequency \( (f_{-3\text{db}}) \) can be increased to 400 MHz, shown in the Figure 2f (green line). The simulated results, therefore, suggest that As-doped In₂O₃ nanowire TTFTs offer great potential in high-frequency device applications. Further optimization of the design toward functional, transparent integrated circuits is in progress.

**Fully Transparent OLED Driving Circuitry.** The ability to fabricate high-performance As-doped In₂O₃ nanowire TTFTs enabled further exploration of transparent circuit applications. Controlling a variable-intensity OLED was selected as the next target. Here a monochrome OLED is wire-bonded on a breadboard together with an As-doped In₂O₃ nanowire TTFT chip (Figure 3). The inset of Figure 3a shows the circuit diagram of the experimental setup, where one TTFT is connected to an external OLED, and \( V_{dd} \) is applied to drain of the transistor. By controlling \( V_{in} \) that provides a gate voltage for the transistor with fixed \( V_{dd} \), the voltage drop across the OLED can be controlled. Figure 3a shows the current flowing through the OLED, which is successfully modulated via \( V_{in} \) by a factor of \( \sim 300 \), thus controlling the OLED light intensity, as shown in Figure 3b. OLED light intensity

![Figure 3](Image)

**Figure 3.** (a) Plot of the output current through the loaded phosphorus OLED \( (I_{OLED}) \) versus \( V_{in} \) with \( V_{dd} \) at 5.0 V in linear scale (red line) and log scale (blue line), respectively. Inset: Circuit diagram of an OLED driven by a transparent As-doped In₂O₃ nanowire transistor. (b) OLED light intensity versus \( V_{in} \) with \( V_{dd} = 5.0 \) V. Inset: OLED spectrum. (c) Optical images of the OLED under \( V_{in} = -3.0, 0.0, \) and 3.0 V.
below 1 Cd/m² is usually defined as the off-state and above 1 Cd/m² as the on-state. Although the present off-state/on-state light intensity ratio is ~5, the effect is clearly visible in Figure 3c, where the OLED is operated with $V_{\text{in}} = -3$ (left), $0$ (middle), and $3$ (right) V.

AMOLED Display and Drive Circuitry. The discussion above demonstrates the high-performance characteristics of As-doped In$_2$O$_3$ nanowire/SAND TFTs, including high device mobility and fast device operation, and can be employed as switching and driving transistors in an AMOLED display circuitry. Here, we go one step further to fabricate an AMOLED display using high-performance As-doped In$_2$O$_3$ TFTs based on our earlier collaborative results on AMOLED display fabrication together with our cooperators and colleagues at Purdue University. Figure 4a shows the equivalent circuit diagram of seven-segment AMOLED display circuitry. Note that the driving circuit of each OLED pixel consists of one switching transistor (T1), one driving transistor (T2), and one storage capacitor (Cst). T1 is employed to select a specified pixel and transfer data through the data line to the OLED. T2 is employed to control the current supplied to the OLED pixel, which is adjusted by controlling the $V_g$ of T2, equal to the voltage difference between the ends of Cst. The storage capacitor is employed to store data during one period for time-varying operations. The EL opening area of each segment is $0.18$ mm².

AMOLED display fabrication begins by patterning the OLED ITO anode and individually addressed bottom gate electrodes by photolithography and wet etching. Next, 50 nm ALD Al$_2$O$_3$ is deposited on the patterned ITO gate and OLED anodes. Following Al$_2$O$_3$ deposition, contact holes above the OLED anodes, as bottom gate electrode contacts for each pixel, are fabricated through a wet etching process. After that, a suspension of As-doped In$_2$O$_3$ nanowires in 2-propanol alcohol is dispersed on the device substrate. A thin layer of source and drain electrodes (T2), and one storage capacitor (Cst). T1 is employed to select a specified pixel and transfer data through the data line to the OLED. T2 is employed to control the current supplied to the OLED pixel, which is adjusted by controlling the $V_g$ of T2, equal to the voltage difference between the ends of Cst. The storage capacitor is employed to store data during one period for time-varying operations. The EL opening area of each segment is $0.18$ mm².

Figure 4. Application of As-doped In$_2$O$_3$ nanowire TFT circuitry to drive a seven-segment AMOLED display. The phosphorus OLED structure is ITO/NPD/CBP:8% Irppy/BCP/LiF/Al. Details can be found in the Supporting Information. (a) Schematic of a seven-segment digit of AMOLED pixel, which consists of one switching transistor (T1), one driving transistor (T2), and one storage capacitor (Cst). The bias conditions to operate the circuit are $-5$ to $5$ V of scan line to full turn-off and turn-on, varying $-5$ to $5$ V on the data line, $3$ V on the $V_{\text{in}}$ line, and $0$ V on the cathode line. (b) Optical photograph of fully transparent AMOLED display before OLED layer deposition with the substrate area marked with a yellow frame for clarity. The feature on the background picture is clearly visible. (c) Optical photograph of AMOLED animation. The seven-segment digit displays numbers 1, 3, and 6, respectively.
(20 nm Al) is then deposited by e-beam evaporation and patterned by lift-off. Following source and drain electrode patterning, a 200 nm thick SiO2 layer is deposited by e-beam evaporation to passivate the device and planarize the nanowire transistors for OLED fabrication. The detail of OLED deposition can be found in the Supporting Information.

Figure 4b shows an optical image of a 1 in. × 1 in. AMOLED display substrate before OLED deposition, with a background image visible through the display region. The optical transmittance spectrum (Figure S3 in the Supporting Information) reveals that the optical transmittance values of the AMOLED display before and after OLED layer deposition are ~81% and ~35% in the visible region, respectively. The optical transmittance should be readily increased using a more transparent OLED design. The display consists of 12 seven-segment OLED pixels, 84 OLED unit pixels, and 156 nanowire TTFTs. For each seven-segment OLED pixel, the scan lines for all unit pixels are individually controlled, as are the data lines. Figure 4c shows optical images of the seven-segment pixels with different numerical digits at different data line voltages (V_{data} = -5 to 5 V) with different scan line voltages (V_{scan} = -5 to 5 V) and fixed V_{dd} (= 3 V). To the best of our knowledge, this is the first demonstration of a seven-segment AMOLED display driven entirely by TTFT circuits.

In summary, we have demonstrated the great potential of As-doped In2O3 nanowires for high-performance transparent electronics. With the aid of arsenic dopants and a self-assembled gate nanodielectric, As-doped In2O3 nanowire TTFTs with transparent ITO contacts show good transparency and excellent transistor performance such as high mobility, high on/off ratio, low operation voltage, and steep subthreshold slope. A saturation device mobility of 1490 cm^2 V^−1 s^−1 is achieved on glass substrates, which is the highest TTFT device mobility reported so far. We further examined the AC gain from a single As-doped In2O3 nanowire TTFT, and the results indicate good frequency response and a unity-gain frequency of 18.8 GHz. In addition, the TTFTs were further utilized to construct a transparent circuit and used to control a variable-intensity OLED. Moreover, an AMOLED display with good transparency was also fabricated which generates numerical displays. Our results suggest that As-doped In2O3 nanowires have great potential to serve as building blocks for future transparent electronics.

METHODS

As-Doped In2O3 Nanowire Synthesis. Ten nanometer gold nanoparticles were dispersed on a Si/SiO2 substrate and utilized as catalysts in the nanowire synthesis. The substrate was then placed into a quartz tube at the down stream end of a furnace, while an InAs target was placed at the upper stream of the furnace. During the laser ablation process, the chamber was maintained at 760 Torr, 700 °C with a constant flow of 150 standard cubic centimeters (scm) of Ar mixed with 10% H2. The typical reaction time was about 50 min. After cooling, the samples were characterized using FESEM, TEM, XRD, and EDS.

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Supporting Information Available: Fabrication details for TTFTs and AMOLED. Electrical and optical data figures for TTFTs. This material is available free of charge via the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

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