Physiological Measurement

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Current-conveyor-based wide-band current driver for electrical impedance tomography

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Abstract
Objective: In this paper a wide-band integrated current driver for electrical impedance tomography (EIT) is presented. The application is primarily for prostate and breast cancer detection which require the tissue to be interrogated at frequencies up to 10 MHz while achieving low harmonic distortion and high accuracy. Approach: The current driver is based on current conveyor architecture and can deliver 1.2 mA of peak to peak ac current between frequencies of 100 Hz–10 MHz. It is fabricated in CMOS 0.18 µm technology with a power supply of 3.3 V, and occupies a core area of 0.26 mm². Main results: The measured harmonic distortion for a peak current of 1.2 mA is <0.1% for frequencies less than 100 kHz, and increases to 0.68% at 10 MHz. The measured output impedance of the current driver is 101 kΩ at 1 MHz and 19.5 kΩ at 10 MHz. Significance: The circuit is suitable for high frequency active electrode applications.

1. Introduction

Bio-impedance varies widely between cancerous and benign tissues and exhibits frequency-dependent characteristics which have been used for differentiating various kinds of cancer (Saulnier et al 2001). Electrical impedance tomography (EIT) is an imaging modality that incorporates the bio-impedances of various parts of the measured tissue to provide a spatial mapping of the organ being probed. By injecting a sinusoidal current into the tissue at the source electrode and measuring the voltages induced at the remaining electrodes, impedance of tissue is obtained, as shown in figure 1. One of the key advantages of an EIT system is its relatively smaller size and inexpensive cost compared to other imaging techniques such as magnetic resonance imaging (MRI) or computerized tomography (CT). Importantly, EIT is also non-ionizing.

A major challenge of EIT is that it requires an accurate, high-output impedance current driver to deliver a pure sinusoidal signal to the tissue being interrogated. The EIT current driver has traditionally been implemented as a Howland current source with discrete components (Tucker et al 2013). This implementation unfortunately introduces a significant amount of parasitic capacitance, which limits the bandwidth of the EIT system. To achieve higher frequencies of operation, the current driver must be implemented in an integrated circuit (IC), as part of an active electrode system, whereby the electronics are physically close to the electrodes and parasitic capacitance is minimized. Several promising IC current drivers have recently been proposed (Yan et al 2011, Constantinou et al 2014, 2015, Hong et al 2015, Kim et al 2017, Wu et al 2018). Unfortunately, none of the solutions reported in the literature have measured operation beyond the 1 MHz range, where electrical impedance interrogation of intracellular physiology could provide increased contrast between benign and cancerous tissue (Jossinet 1998, Halter et al 2008). Also, none of the previous implementations are designed to drive a DC blocking capacitor, which is necessary for patient safety in EIT measurements (Lionheart et al 2001, McEwan et al 2007).

In this paper, a wide-band, current-conveyor-based, integrated CMOS current driver is introduced. Compensation for high-speed operation at the transconductance stage is achieved using the indirect compensation technique (Satxena 2007) which enables operation up to 10 MHz. Also, current-mode circuits (Wilson 1990) at the output stage further aid in the wide-band operation of the designed current driver. Finally, a DC servo-loop circuit at the output branch maintains reliable operation of the current driver in the presence of a DC blocking capacitor at the current injection electrode.
2. Overview

Our proposed current driver for this design is based on the CCII current conveyor (Sedra and Smith 1970) shown in figure 2. The input to the current driver is the voltage, $V_X$. This is buffered to $V_X$, which generates a current $I_X = \frac{V_X}{R_X}$ through the load resistor $R_X$. The current $I_X$ is mirrored to the output of the current-controlled current source, and $I_Z = I_X$ flows through a DC-blocking capacitor, $C_{\text{block}}$, to an electrode and into the tissue. Our current driver architecture (figure 3) is based on the work presented in Jivet and Dragoi (2008). We modified the original architecture to make it suitable for high frequency EIT applications. In particular, we designed the two-stage operational amplifier (op-amp) of figure 3 with indirect compensation around a class AB control circuit, to enable current interrogation frequencies up to 10 MHz. Also, we implemented a DC-biasing servo loop at the output of the current driver; this ensures proper operation of the current driver in the presence of a 1 μF DC-blocking capacitor that is necessary for patient safety.

3. Circuit design and analysis

Details of the circuit implementation are presented in this section.

3.1. V-I conversion

Figure 4 shows the circuit diagram of the two-stage op-amp with indirect compensation technique used for the voltage to current conversion in the current driver. A RHP pole zero appears in the transfer function of a conventional two-stage op-amp compensated using a compensation capacitor $C_c$. This problem has been well-studied (Baker 2010) and various compensation techniques exist to cancel the RHP zero or move it into the LHP to improve stability. However, the nulling resistor technique for compensation is process dependent and the use of a transistor in triode region of operation can cause issues with large signal behavior (Baker 2010). Also, the value of compensation capacitor selected limits the speed of the circuit when high frequency of operation is desired.

In the indirect compensation technique, the compensation capacitor is not directly connected to the op-amp output. Instead, pole-splitting is achieved indirectly using a common gate transistor, $M_{cg}$, feeding the current from the output back to the first stage. Input transistors $M_{02}, M_{3}$, with current mirror loads $M_{6}, M_{7}$ and cascaded tail transistors $M_{0}, M_{1}$ form the input stage of the two stage op-amp. The gain of the input stage is given by $A_{v1} = g_{m2}(r_{o3}||r_{o5})$, where $g_{m2} = g_{m3} = g_{M1}$ are the transconductances of the input differential pair and $r_{o3}, r_{o5}$ are the output impedances of transistors $M_{3}, M_{1}$ respectively. The branch comprising of transistors $M_{6}, M_{8}, M_{9}$, and $M_{g}$ form the indirect compensation branch in the circuit along with the compensation capacitor $C_c$. The gate of the common gate transistor $M_{cg}$ is tied to the common mode voltage of the circuit. The currents in the input differential pair transistors and the indirect feedback branch are kept equal to achieve $g_{m1} = g_{m2}$. The output branch which consists of the second stage gain is provided by transistors $M_{10}$ and $M_{13}$ which is the current source load. The gain is given by, $A_{v2} = g_{m10}(r_{o10}||r_{o13})$, where $g_{m10}$ is the transconductance of transistor $M_{10}$ and $r_{o10}, r_{o13}$ are the output impedances of transistors $M_{10}, M_{13}$ respectively. The bias voltages $v_{m1}$ and $v_{m2}$ are provided using a wide swing cascade current mirror (Caruso et al 2012) (not shown). Class AB output buffer stage is formed by transistors $M_{11}, M_{12}, M_{14}$, and $M_{15}$. When voltage, $V_1$, at the gate of transistor $M_{10}$ increases, $M_{15}$ turns on and $M_{14}$ turns off, as the gates of $M_{11}$ and $M_{12}$ move towards GND. Similarly, $M_{14}$ sources all the current
Figure 2. Block diagram of the current conveyor architecture (Sedra and Smith 1970). Current is generated at terminal X using an on-chip resistor such that $I_X = \frac{V_Y}{R}$, and $V_X$ follows the voltage at terminal Y. Current $I_X$ is delivered to terminal $Z$ with a current gain of unity.

Figure 3. The architecture of the current driver. (a) The voltage to current conversion is performed using a two-stage op-amp with indirect feedback compensation. (b) Class AB output stage at the output of the op-amp is necessary for generating the sinusoidal current at terminal $X$ using a resistor $R_X$. (c) Current is mirrored to the high output impedance terminal $Z$ with a gain enhanced current mirror forming the output stage.

Figure 4. Two-stage op-amp with indirect compensation followed by a class AB output stage. (a) The current from the output node $Z$ is indirectly fed to node $1$ using the common gate transistor $M_{14}$. This forms the indirect feedback compensation technique. (b) Transistors $M_{13}, M_{23}, M_{14}, M_{15}$ form the class AB output stage to source and sink currents into node $X$. Gate voltages, $V_{os1}$ and $V_{os2}$ are set by gate biasing circuits (not shown).
when $v_1$ decreases, which implies a class AB operation. The current source $i_{eb}$ provides the necessary DC current bias for the class AB output branch.

Compared to conventional frequency compensation techniques, the indirect compensation technique uses smaller capacitors (Saxena 2007). The reduced footprint allows multiple current drivers to be integrated onto a single chip; this avoids the parasitic capacitance that would be experienced by a single, multiplexed current source (Saulnier et al 2001).

### 3.2. Gain boosted cascode output stage

The high output impedance necessary for the current driver is achieved by using the structure shown in figure 5. The gain boosting amplifier in figure 5 should have high unity gain frequency and exhibit single pole behavior to ensure stability. To achieve this we implement the amplifier as a common source amplifier with a current source load (transistors $M_{S6}$ – $M_{S1}$ of figure 6). Gain boosting is similarly implemented for the PMOS half of the output branch, using transistors $M_{16}$ – $M_{33}$. The low frequency small signal gain of the PMOS and NMOS gain boosting amplifiers is given by the following equations (Zeki and Kuntman 1997):

\[ A_{pb,P} = g_{m21}(r_{o21}||r_{o21}) \]  

\[ A_{pb,N} = g_{m29}(r_{o29}||r_{o31}) \]

where $g_{m21}$, $g_{m29}$ are the transconductances of transistors $M_{S1}$, $M_{S2}$ respectively and $r_{o21}$, $r_{o23}$, $r_{o29}$, $r_{o31}$ are the output impedances of transistors $M_{S1}$, $M_{S2}$, $M_{S9}$, $M_{S1}$ respectively. From equations (1) and (2), the overall output impedance at node $Z$ is given as

\[ Z_{out} = (g_{m25}r_{o25}g_{m21}(r_{o21}||r_{o23})) || (g_{m33}r_{o33}g_{m29}(r_{o29}||r_{o31})). \]

### 3.3. Output DC servo-loop

In EIT applications, a DC blocking capacitor at the output of the current driver ensures that no DC current flows into the human tissue (Lionheart et al 2001). This results in an equivalent structure at the output stage of the current driver as shown in figure 7. Mismatch in the DC values of $i_{p mos}$ and $i_{n mos}$ will cause the output node $Z$ to rail to either $V_{DD}$ or GND. To avoid this, and to maintain a suitable DC bias voltage at node $Z$, we use the servo-loop circuit shown in figure 8. Here the output branch of the current driver is shown where an operational transconductance amplifier (OTA) sets the output voltage to $V_{CM}$, which is typically at 1.65V. The OTA is implemented as a current mirror OTA with input transistors sized to minimize the capacitive loading at node $Z$. The high output impedance of the OTA along with the capacitor $C_{EXT}$, external to the ASIC, forms a low-pass circuit. In the designed circuit $M_{PB}$ is 1/30 times the width of transistor $M_{S3}$, while the length remains the same. Its loading effect at the drain of transistor $M_{S3}$ is negligible. The designed servo-loop circuit sets the output branch at a reliable operating voltage such that the cascode transistors in the output branch have sufficient headroom for reliable operation.

### 4. Measured results

The current driver was fabricated in XFab 0.18 μm XH018 CMOS process with supply voltage of 3.3V. Design, layout and simulation was performed using Virtuoso Cadence. The resistor $R_X$ of figure 3 was implemented as a 500 Ω resistor, integrated on the ASIC. Two additional current driver test structures were also designed and included in the chip for complete measurement. The current driver core area with test structures is approximately 0.26 mm² as shown in figure 9.
4.1. Harmonic distortion
The input signals to the current driver were generated using a Keithley Instruments 3300 waveform generator capable of generating sinusoidal signals greater than 10 MHz with negligible distortion contributing to the measurements. A 600 mV peak to peak voltage at the input terminal Y generates the maximum current of 1.2 mA at terminal Z. The output voltage at the load was monitored using a Rigol 1104-Z oscilloscope. Figure 10 shows the measured THD values against frequencies. Current values of 1 mA, and 1.2 mA are chosen to show the performance of the current driver with a 500 Ω load. The current driver achieves a THD of less than 0.7% harmonic distortion at 10 MHz while delivering a current of 1.2 mA to the load.

4.2. Noise
A Stanford Research Systems SRS 785 spectrum analyzer was used for noise measurements of the current driver. Due to limitations of the equipment, noise was measured up to 100 kHz. Figure 11 shows a comparison of
measured noise with respect to Cadence simulations. The total integrated noise at the output was approximately 658 \mu V determined by simulation.

4.3. Output impedance

The measurement of the output impedance of the current driver was performed as described in Cook et al (1994). The test configuration uses a Linear Technology LT1806 wide bandwidth precision op-amp as a negative feedback amplifier. To obtain accurate measurements, we used calibration and feedback resistors with tolerance of 0.1%. The associated parasitics of the board were measured using an Instek 821 precision LCR meter. The measured board parasitics, along with the output pad capacitance of the chip (terminal Z), were incorporated into the calculation of the output impedance. An average of 2500 points for a single frequency point measurement was used to obtain reliable measurement data. Figure 12 shows the output impedance versus frequency for the current driver. The output impedance is 101 k\Omega at 1 MHz, and 19.5 k\Omega at 10 MHz.

4.4. Cole–Cole plots and accuracy

The suitability of the designed current driver for complex impedance measurements up to 10 MHz was verified with the setup shown in figure 13. An R–C circuit combination was used to model the complex tissue impedance of the breast (Halter et al 2008). A peak-to-peak input voltage of 500 mV was fed from the signal generator such
that 1 mA\textsubscript{pp} of current was injected into the load. A 100 Ω sense resistor with 0.1% tolerance was included at the output to measure the accurate current from the current driver. The voltage across the sense resistor was captured by the data acquisition system. A digital matched filter in MATLAB was then used to extract the amplitude and phase of the complex load. The value of the passive components used in the setup was measured using an LCR meter and incorporated into the accuracy calculations. An average of 50 measurements was performed for each frequency point to obtain accurate results. The measured Cole–Cole plot for the complex impedance setup is shown in figure 14.

4.5. Saline tank measurements
To illustrate the functioning of the current driver in a full EIT system, saline tank experiments were performed to obtain impedance images. The architecture of the 16-electrode EIT system is shown in figure 15. An ASIC
Figure 12. Output impedance versus frequency for the current driver. The measured output impedance is 10.1 kΩ at 1 MHz, and 19.5 kΩ at 10 MHz.

Figure 13. Setup for current driver testing. Input signal is fed by a signal generator and the voltage across the sense resistor is captured by the data acquisition system. Amplitude and phase extraction is performed in the digital domain with a matched filter.

Figure 14. Cole–Cole plot for a parallel R-C load shown in figure 13 to model the complex tissue impedance.
Figure 15. Architecture of the EIT system. An ASIC which includes the current driver, IA, VGA, and ADC, implements the core EIT functionality and is included on the daughter-board module with required voltage references, current biases and switch configuration ICs. The daughter-boards are mounted on the motherboard with I/O connectors. The FPGA on the motherboard is responsible for control, data acquisition, and communication. The data from the FPGA is sent to the MATLAB software on the computer to form impedance matrices and reconstruct images.

Figure 16. Saline tank setup and reconstructed image. (a) Brass rod of 1.3 cm diameter placed at the center of the saline tank with water depth of 1.27 cm and conductivity 1000 µS cm⁻¹. (b) Reconstructed image for the saline tank setup.
was designed with circuits such as the current driver, instrumentation amplifier (IA), variable gain amplifier (VGA), analog-to-digital converter (ADC) and switches which implement majority of the EIT functionality. Daughter-board modules include the ASIC with voltage references, biasing, switching mechanisms, power and serial interfaces. A motherboard houses the daughter-board modules along with an FPGA carrier board, and peripheral components. The FPGA controls the various SPI interfaces and acquires the digital data in parallel from all the channels on the daughter-board modules. Digital matched filter was implemented on the FPGA fabric to extract the in-phase and quadrature component of voltages to reduce the data throughput from the hardware. Computed data was sent to the MATLAB software on a computer to generate impedance matrix and obtain reconstructed images. Difference imaging was performed with a standard Gauss–Newton algorithm using Laplace–smoothing Tikhonov regularization.

An 8.5 cm diameter tank was filled with a saline solution of conductivity 1000 μS cm⁻¹ which is in the range of value reported for different breast tissues (Jossinet and Schmitt 1999). The tank was fitted with conductive polymer plugs in contact with alligator clip electrodes attached to the tank. The spacing between electrodes was 3.25 cm. An initial experiment consisted of filling the tank with saline to a height of 1.27 cm to form a baseline measurement. Subsequent experiments were performed with a brass rod of diameter 1.3 cm placed at the center of the saline tank. Two hundred and forty current source-sink patterns were used to obtain data from the designed 16-electrode EIT system. The image obtained from the saline tank experiment using reconstruction algorithms (Murphy et al 2017) is shown in figure 16.

5. Discussion

The reduction in the output impedance can be attributed to the placement of the output port of the current driver in the ASIC. Adjacent pads increase the capacitive coupling, and degrade the high frequency measurements. The estimated parasitic capacitance of the ASIC pads is ~3.5 pF and this value is consistent with the measured results (at lower frequencies). A future iteration of the ASIC will isolate the adjacent pads to obtain improved measurement of the output impedance.

The impedance values for cancer (CA), mammary gland (MA) and fibroadenoma (FA) tissues for breast, at 1 MHz are 139, 69, and 17.4 Ω respectively (Jossinet 1996, Murphy et al 2017). Similarly for prostate, impedance values for cancerous (CP), and glandular (GI) tissues at 10 MHz are 145 and 118 Ω respectively (Halter et al 2008, Wan et al 2010). Thus, the output impedance of the current driver at 101 kΩ at 1 MHz and 19.5 kΩ at 10 MHz represents an error of less than 0.01% which is well within the accuracy requirement of EIT systems (Halter et al 2008, Rao et al 2018).

The current driver achieves wide-band operation up to 10 MHz, necessary for EIT prostate and breast cancer detection. The THD values achieved are an improvement from previously reported integrated designs. The use of indirect feedback compensation enables wide-band operation with a small compensation capacitor. This is especially helpful when integrating multiple EIT channels on a single ASIC. On-chip bandgap references for biasing would improve the integration of the current driver in building multiple channel EIT systems. Table 1 shows a comparison with previously reported current drivers. None of the current driver implementations reported in the comparison table have measured operation up to the 10 MHz range, where electrical impedance interrogation of intracellular physiology could provide increased contrast between benign and cancerous tissue. A DC blocking capacitor is essential when interfacing with tissue for patient safety and is not included in these implementations. The current driver design presented in this paper has an architecture which addresses these issues.

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Table 1. Measured performance and comparison.

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<tbody>
<tr>
<td>Architecture</td>
<td>Differential current generator</td>
<td>Negative feedback</td>
<td>Differential current generator</td>
<td>Differential current generator</td>
<td>Negative feedback</td>
<td>Current conveyor II</td>
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<tr>
<td>Bandwidth</td>
<td>90 kHz</td>
<td>≤1 MHz</td>
<td>&lt;200 kHz</td>
<td>256 kHz</td>
<td>500 kHz</td>
<td>100 Hz–10 MHz</td>
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<td>Output impedance</td>
<td>&gt;560 kΩ @ 90 kHz</td>
<td>360 kΩ @1 MHz</td>
<td>—</td>
<td>—</td>
<td>1.12 MΩ @ 500 kHz</td>
<td>101 kΩ @ 1 MHz, 19.5 kΩ @ 10 MHz</td>
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<tr>
<td>Maximum output current (peak-peak)</td>
<td>350 μA</td>
<td>1 mA</td>
<td>1 mA</td>
<td>1 mA</td>
<td>6 mA</td>
<td>1.2 mA</td>
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<tr>
<td>THD (current) (frequency)</td>
<td>0.81% (250 μA)</td>
<td>&lt;0.1% (1 mA, 50 kHz)</td>
<td>&lt;0.1% @ 0.1 mA</td>
<td>&lt;0.47% (1 mA, 128 kHz)</td>
<td>&lt;0.18% (6 mA, 500kHz)</td>
<td>&lt;0.14% (1.2 mA, 500 kHz) &lt;0.7% (1.2 mA, 10 MHz)</td>
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6. Conclusion

A CMOS wide-band current conveyor based on current conveyor architecture is presented. High linearity is achieved by the use of a resistor for current generation in the V-I conversion phase, whereas high accuracy is obtained by the use of a gain boosted cascode structure for high output impedance. The design was fabricated in the 0.18 μm process and can deliver 1.2 mA of current up to frequencies of 10 MHz. The above performance is achieved while maintaining harmonic distortion of less than 1% essential for EIT imaging (Rao et al. 2018). A servo-loop circuit is designed for the output branch of the current driver to account for the DC blocking capacitor when injecting current into the human tissue. The current driver specifications have been measured using custom built PCBs and its performance characterized with a complex load impedance up to 10 MHz. A 16-electrode EIT system which incorporates the current driver was used to measure a saline tank setup and an image is obtained. The circuit is intended for use in active electrodes and EIT applications which require high frequency of operation to detect cancerous tissues.

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