Structured Design Methodology to Achieve a High SNR Electrical Impedance Tomography

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Abstract—In this paper, we present a methodology for designing the main circuit building blocks of an electrical impedance tomography (EIT) system. In particular, we derive equations that map system-level EIT specifications to the performance requirements of each circuit block. We also review the circuit architectures that are best suited for meeting a given set of performance requirements. Our proposed design methodology is focused on maximizing the EIT system's signal-to-noise ratio (SNR) while minimizing total power consumption.

Index Terms—Electrical impedance tomography, SNR, matched filter, instrumentation amplifier, ADC, IA, driver, frame rate.

I. INTRODUCTION

Electrical impedance tomography (EIT) is a biomedical imaging technology that is based on the differences in conductivity and permittivity exhibited by different tissue types. In EIT, small, imperceptible AC currents are injected into the region of interest via pairs of electrodes and the resulting “boundary voltages” that develop on the tissue surface are measured [1], [2], [3], [4], [5]. The injected currents and measured boundary voltages are used to reconstruct a tomography-like impedance map of the tissue under test. Compared to other imaging modalities (e.g. X-ray, MRI), EIT is radiation-free, inexpensive and potentially miniaturizable [6], [7], [8], [9].

The challenge with EIT is that the image reconstruction problem is poorly conditioned and ill-posed. So, to generate clinically-useful images, the boundary voltages must be measured with a high signal-to-noise ratio (80-100 dB SNR) [10], [11], [12]. Also, EIT often requires a wide frequency range of operation (say, 100 Hz to 10 MHz), as this allows for frequency-specific tissue interrogation and multi-frequency EIT imaging, both of which improve image quality [13]. To meet these demanding specifications, the state-of-the-art EIT systems are built with discrete, high-performance circuit components and data acquisition modules. Unfortunately, discrete components introduce significant channel-to-channel variation, clock phase errors and shunt parasitic capacitances, all which limit imaging quality at the higher frequencies.

One solution to these issues is to implement the EIT instrumentation as an integrated system-on-chip (SoC) [6], [14], [15]. Such a multi-channel EIT SoC must achieve high SNR, high frequency operation, while minimizing power consumption. Excessive power consumption would require a bulky thermal management system, which would keep the SoC away from the body, necessitating long cables that cause channel cross talk and ultimately degrade the high frequency performance.

In this paper, we provide a structured methodology for designing the individual circuit components that meet system-level EIT performance requirements while minimizing power consumption.

II. RELATED WORK

Many review papers have been published in the EIT literature [16], [17], [18]. The review in [16] mainly studied the development and evolution of EIT hardware. The review paper presented in [17] focused on the main sources of error in multi-frequency EIT systems, without analysis of circuit components. Also, the focus of the work in [18] was to cover the different approaches employed in discrete-type EIT systems, along with some design requirements. However, there is still a need for a procedural design that relates each individual circuit block specification of an EIT ASIC to top-level EIT system requirements. Therefore, in this work we study the EIT chain and derive equations to formulate the design of each individual block, in order to bridge the gap between EIT system level specifications and circuit design requirements. In our analysis, the emphasis is placed on achieving a high SNR EIT, while meeting the frame rate requirement of the system and avoiding components that consume excessive amounts of power.

III. EIT SYSTEM ARCHITECTURE

In order for an image to be taken from a tissue or an organ, different digital and analog blocks need to be employed. A simplified block diagram of a typical EIT system is shown in Fig. 1. The EIT system can be roughly divided into three main subsystems: 1) A current injection block (current driver), 2) a data acquisition block (read-out chain), and 3) a reconstruction algorithm. The synchronization unit generates a reference clock that synchronizes the current injection block with the data acquisition unit, which is necessary for extraction of the amplitude and phase. In order to avoid any delay skews between the main processors and different channels in a multi-channel EIT system, the digital signals must be transmitted differentially, travel equal lengths, and have well-controlled path impedances [19]. This helps to minimize the clock phase delay between different channels. Any remaining
phase differences between the channels can be calibrated [17], [20].

In the rest of the paper, we study and analyze the circuit components of an EIT system: data acquisition and injection blocks. The reconstruction algorithm is out of scope of this work and interested readers are encouraged to read [20], [21], [22], [23].

IV. DATA ACQUISITION BLOCK

A. Matched Filter

In EIT systems, reconstructing an internal conductivity map from boundary voltages is an ill-posed problem. Therefore, the more precise the recorded data, the better the reconstruction results [7]. If measurements lack sufficient SNR levels, an inability to distinguish minute differences between recording electrodes may result. Fortunately, at the end of the signal chain in an EIT system, there is typically a matched filter (as shown in Fig. 1). The matched filter maximizes the SNR of a signal, even if the signal is highly contaminated with White Gaussian noise [24]. Therefore, even with relatively low-precision circuit components, measurements with high SNR values in EIT systems are achievable because of the matched filter [25], [26]. There are two ways to implement the matched filter: digital and analog. In the digital approach, the matched filter is located at the end of the chain, following the ADC. In the analog version of the matched filter, however, the filter comes before the ADC block. Each approach has its own advantages and disadvantages, which have been discussed in the literature, namely [18], [25], [27], and are briefly mentioned in the following.

1) Analog Matched Filter: A block diagram of an analog matched filter is shown in Fig. 2(a), alongside a block diagram of a digital matched filter in Fig. 2(b) for comparison. The input signal, \(X(t)\), is multiplied with the orthogonal signals generated from the reference signal, \(V_{ref}(t)\), where the reference signal has the same frequency as the input signal. In the analog matched filter, the reference signal may be a square wave or a sinusoidal signal. Recent ASIC EIT systems with analog matched filters have employed the square wave reference signal due to the simplicity of implementation [6], [8]. Note that, due to the nature of the square wave, odd harmonics of the input signal can be translated into DC. The low-pass filter (LPF) in the matched filter extracts the in-phase (\(V_I(t)\)) and quadrature (\(V_Q(t)\)) components of the signal. To extract the amplitude and phase, and reconstruct the EIT image, the in-phase and quadrature components must be further processed in the digital domain. Therefore, two ADCs digitize the signals. Note that one ADC can also be time multiplexed between the in-phase and quadrature components. However, this comes with the penalty of increased measurement time. Since the ADC in the analog matched filter only processes a DC signal, the speed requirement of the ADC may be relaxed.

A detailed analysis of the analog phase sensitive detectors can be found in [25], [27]. Furthermore, the SNR of the in-phase component in the presence of thermal noise has been calculated in [25]. However, we are most interested in the amplitude and phase SNRs of the matched filter. In order to analyze the amplitude and phase SNRs in the presence of an ADC, we derived the following [25]:

\[
\text{SNR}_A = 10 \log_{10} \left( \frac{A^2}{\sigma_n^2 \left( \frac{2BW_f}{BW_n} \right) \left( \frac{1}{N} \right) + \frac{\text{LSB}^2}{12}} \right) \tag{1}
\]
where LSB is the least significant bit of the ADC, and \( A \) is the amplitude. The noise of the current injection block, \( I_A \), and the analog components of the matched filter are combined and modeled at the input of the matched filter with a total power of \( \sigma_n^2 \). The equivalent noise bandwidth is represented by \( BW_n \), which is due to the filtering effect of the op-amp preceding the ADC. \( BW_F \) is the equivalent noise bandwidth due to the low-pass filter. \( BW_F \) is equal to the low-pass filter’s 3-dB frequency, multiplied by some factor, \( \pi/2 \geq k \geq 1 \), which depends on the filter order. For the sake of simplicity, we will assume this factor is equal to unity. In our calculations, similar to what was suggested in [25], we assume that the equivalent noise bandwidth is \( f_m \leq BW_n < 3f_m \), and the equivalent bandwidth of the low-pass filter, \( BW_F \), is less than \( f_m \). The noise is spread over \( BW_n \), with a power spectral density of \( \sigma_n^2/BW_n \). The ADC takes \( N \) samples of the DC signal, with \( b \) bits of resolution and a quantization noise power of \( \text{LSB}^2/12 \). These samples are then averaged in a processor to calculate the amplitude. The averaging process helps to reduce the noise (to be explained later).

Similarly, the phase SNR can be written as:

\[
\text{SNR}_\phi = 10 \log_{10} \left( \frac{\phi^2 A^2}{\sigma_n^2 \left( \frac{2BW}{BW_n} \right) \left( \frac{1}{N} \right) + \text{LSB}^2 \frac{2}{12}} \right) \tag{2}
\]

where \( \phi \) is the phase.

For instance, to provide 80 dB SNR in the amplitude measurement of a 10 kHz signal with the thermal noise, \( \sigma_n \), of 1 mVrms, an analog matched filter can be built with the following components: a low-pass filter with a 210 Hz cutoff, and a 50 kilo-samples per second, 14-bit ADC.

The low sample-rate ADC makes this analog matched filter design an attractive one. However, it comes with the price of a long acquisition time, which comprises the settling time of the low-pass filter and time it takes to collect enough samples to perform an I/Q extraction.

To achieve an accuracy of Acc dB, the minimum settling time required for transients to die out in a low-pass filter with the equivalent bandwidth of \( BW_F \) is given by:

\[
t > \ln \left( \frac{10^{(\text{Acc}/20)}}{2\pi BW_F} \right) \tag{3}
\]

Assuming a desired accuracy of 60 dB, the settling time for our example 210 Hz low-pass filter is at least 5.23 ms. After the transients settle, it takes an additional 0.1 milliseconds for the ADC to collect the 5 samples that must be averaged to produce the \( V_I \) and \( V_Q \) values, from which the signal amplitude can be calculated.

2) Digital Matched Filter: In the digital approach, the input signal \( X(t) \) (in Fig. 2(b)) is digitized immediately, such that the quadrature/in-phase mixing and filtering operations are performed in the digital domain.

We previously presented an analysis of the SNR that may be achieved using a digital matched filter, with a given amount of input thermal noise and a given ADC resolution and frame rate [28]. For the sake of simplicity, we assume the thermal noise is more than \( \sim 15\% \) of an LSB of the ADC, such that we can use the simplified continuous-uniform SNR model for extracted amplitude and phase [28]:

\[
\text{SNR}_A = 10 \log_{10} \left( \frac{A^2 \left( N/2 \right)}{\text{LSB}^2/12 + \sigma_n^2} \right) \tag{4}
\]

\[
\text{SNR}_\phi = 10 \log_{10} \left( \frac{A^2 \left( N/2 \right) \phi^2}{\text{LSB}^2/12 + \sigma_n^2} \right) \tag{5}
\]

where \( A \) is the amplitude, \( N \) is the number of taps of the matched filter (the number of samples the matched filter processes), and \( \phi \) is the phase of the signal. The power of the quantization noise of the ADC is \( \text{LSB}^2/12 \), and the LSB for a \( b \)-bit ADC is defined by \( \text{LSB} = V_{FS}/2^b \), where \( V_{FS} \) is the full-scale voltage, and \( \sigma_n^2 \) is the variance of the thermal noise modeled prior to the matched filter.

In evaluating the amplitude SNR in (4), one notes that there are three distinct ways to achieve a higher SNR: 1) by increasing the number of taps of the matched filter, 2) by reducing the total noise in the chain, and 3) by increasing the resolution of the ADC. The impact of each of these choices will be studied in the following sections.

In comparing the SNR equations (1) and (4), one notes the following fundamental differences: 1) averaging in the digital matched filter reduces both the quantization and thermal noises, whereas only the thermal noise is reduced in the analog implementation, and 2) trade-off between \( BW_F \) (long settling time) and higher SNR in the digital matched filter.

Here, we perform a side-by-side comparison of the costs of achieving high SNR EIT using analog versus digital matched filters. Let us assume that the target SNR is 80 dB, with an input signal of 10 kHz, and a thermal noise, \( \sigma_n \), of 1 mVrms.

The analog matched filter must employ an ADC with a resolution greater than 13 bits (>80 dB); therefore, a 14-bit ADC was chosen. In order to achieve an acceptable settling time, we selected an eighth-order filter with a cut-off frequency of 8.4 kHz and a settling time of around 200 \( \mu \)s. By plugging these values in (1) and assuming a noise bandwidth equal to \( f_m \), \( N \) must be equal to 210. If, after the settling time has passed, the \( N \) samples are captured in one period of the input signal, the ADC sampling frequency is equal to 2.1 MHz (210×10 kHz). The total processing time is thus equal to 300 \( \mu\)s (=200 \( \mu\)s + 1/\( f_m \)).

In contrast, in the digital matched filter, the SNR of the ADC does not need to be higher than the target EIT SNR. Therefore, we selected a 10-bit ADC. By plugging these values into (4), \( N \) for the digital matched filter must be equal to 264. Dedicating the same processing time (300 \( \mu\)s) to the digital matched filter, mandates an ADC with a sampling frequency of 880 kHz (=264/300 \( \mu\)s). A summary of this comparison is shown in Table 1. As can be seen, to achieve a high SNR of 80 dB, the analog matched filter requires a 14-bit, 2.1 MHz ADC. To achieve the same level of SNR in a digital matched filter, a 10-bit 880 kHz ADC can be employed, illustrating that implementation of a digital matched filter is more power efficient. In terms of chip area, it is shown in [29] that at low values of SNR, analog computation is cheaper and less area consuming compared to digital implementation. However,
TABLE I
COMPARISON BETWEEN ANALOG AND DIGITAL MATCHED FILTERS

<table>
<thead>
<tr>
<th></th>
<th>Analog Matched Filter</th>
<th>Digital Matched Filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Filter Order</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>Analog Filter Bandwidth</td>
<td>8.4 kHz</td>
<td>2.8 kHz</td>
</tr>
<tr>
<td>ADC Resolution</td>
<td>14 bits</td>
<td>10 bits</td>
</tr>
<tr>
<td>Sampling Frequency</td>
<td>2.1 MHz</td>
<td>880 kHz</td>
</tr>
<tr>
<td>Potential ADC Architecture</td>
<td>Delta-sigma</td>
<td>SAR</td>
</tr>
</tbody>
</table>

Matched filter design requirements to achieve an EIT system SNR of 80 dB with a processing time of 300 µs. We have assumed a 10 kHz input frequency and 1 mVrms thermal noise (referred to the input of the matched filter). Also, the low-pass filter in the analog matched filter is assumed to be eighth-order with a bandwidth of 8.4 kHz.

at high SNR levels, demand for accurate analog circuitry mandates low-noise precise analog components that translate to higher power consumption when compared to the digital equivalent.

B. Instrumentation Amplifier

For SNR considerations, the most relevant specification of the instrumentation amplifier (IA) is noise. However, common mode rejection ratio (CMRR) is also an important feature to consider due to its effect on measurement accuracy.

1) Common-mode Rejection Ratio: The common-mode voltage that the IA measures can be divided into three main parts: half-cell potential, mean body voltage, and current-caused induced voltage. The half-cell potential is a DC voltage that develops at the electrode-skin interface, and is on the order of 223 mV for an Ag/AgCl electrode [30]. The mean body voltage is the mean voltage of the body with reference to ground. Referring to Fig. 3, any mismatch between the two current sources must flow to ground through the input impedance of the IA, or through any reference electrode, which results in a mean body voltage. The current-caused induced voltage is an intentional voltage induced due to the current injection pattern, shape and electrode placement, which exists between two electrodes referenced to the mean body voltage [31]. As such, the current-caused induced voltage is a common-mode signal that occurs at the same frequency as the differential electrode voltage.

The presence of the common-mode signal can deteriorate the accuracy of the measurements, and potentially saturate the chain. The differential (desired) signal on the recording electrodes can be comparable or smaller than the common-mode (undesired) signal. Therefore, the IA gain intended to amplify the small differential signal can saturate the chain due to the large common-mode signal. Furthermore, any imbalance in the chain can translate the common-mode signal into a differential signal, introducing error to the measurements.

An IA relies on two techniques to achieve common-mode rejection. The first, balancing, maintains the same level of common-mode signal in both halves of the differential signal path. The second, isolation, prevents the common-mode signal from propagating beyond the IA’s input stage.

Balancing depends on keeping the differential signal path well-matched. If both halves of a differential signal are processed identically, then taking their difference will cancel out any common-mode noise. The common-mode signal in EIT, in contrast to bio-potential measurements systems, occurs at the same frequency as the input signal. This can include some relatively high-frequency content [31], [32]. Therefore, the matching requirement applies not only to transistors and drawn passive components, but also to parasitic capacitances. A careful, symmetric layout can reduce parasitic mismatch, but non-idealities in the fabrication process, along with practical routing constraints, means that there will always be some mismatch in the signal paths, particularly at higher frequencies. One solution is to trim out imbalances with laser trimming or programmable devices. This approach is costly, but can improve CMRR by 20 dB [32].

Isolation, either active or passive, confines the common-mode signal to the input stage, while allowing the differential

Fig. 3. Circuit model of a bio-impedance measurement to illustrate the common-mode voltage. The subindexes csr and csi refer to the current source and sink, respectively. $Z_{ei}$ and $Z_{er}$ are respectively the injecting and recording electrodes and the impedance of tissue is modeled as $Z_T$. The common-mode impedance of the IA is modeled with $Z_c$, which is made of a high resistance in parallel with a shunt capacitance. $Z_d$ also represents the differential-mode input impedance of the IA.

Fig. 4. Illustration of the active isolation technique employed by current conveyor-based IAs. This works by buffering the input voltages and converting their difference to a resistor current, which is then processed by the subsequent stages of the IA. This helps to confine the common mode voltage to the input stage buffers (left side of the red dashed line shown in the figure).
mode signal to propagate through the rest of the IA. This way, any mismatch that is encountered after the input stage will have no effect on CMRR. Low-frequency common-mode signals can be isolated with AC coupling capacitors (passive isolation), but high frequency signals require the active isolation provided by a current conveyor-based IA [33]. Active isolation works by buffering the input voltages and converting their difference to a resistor current, which is then processed by the subsequent stages of the IA (Fig. 4). By taking the difference of the input voltages, any common-mode signal is canceled out and is effectively confined to the input stage buffers. Successful isolation depends on proper matching of these input stage buffers. This can be achieved by ensuring that the buffers have a high closed-loop gain accuracy, a quantity that is improved as open-loop gain is increased. One buffer implementation that provides a high loop gain is the flipped source follower, as used in [34]. To achieve even higher values of open loop gain (and hence better closed-loop gain accuracy and matching), the input stage buffers can be implemented with gain-boosted super source followers [35], [36], as shown in Fig. 5. The challenge with the gain-boosted super source follower is that it is prone to instability. This is typically addressed with a compensating capacitor, which in turn requires a large amount of current to charge/discharge at a high-enough rate to meet bandwidth requirements [36]. The extra power consumption is the cost of rejecting common-mode signals that are within the operating frequency of the EIT signal.

2) Noise Budget of the IA Block: Figure 5 shows an implementation of the current conveyor-based IA structure. The input transistors \( M_{1,2} \) and the resistor \( R_l \) are dominant sources of noise. To reduce noise, one may increase the transconductance of the input transistors and/or reduce \( R_l \). An increase in the transconductance involves an increase in the size and/or current of the transistor, both of which are costly in terms of power and area. Furthermore, the value of \( R_l \) must be as small as possible to reduce noise. However, small resistors require higher currents that need to be provided by \( M_{3,4} \), which result in more power consumption. Therefore, a trade-off must occur between the generated noise and dissipated power.

In section IV A, SNR equations were provided that include the maximum noise that can be tolerated in the chain, when the noise is referred to the input of the instrumentation amplifier. We can assume that in the EIT chain, the injection block, the instrumentation amplifier, and the ADC driver generate the majority of noise. Therefore, the noise budget may be divided between these three blocks.

By rearranging the digital matched filter equations, Eqs. (4) and (5), one can find the maximum tolerable noise in the chain with regard to the extracted amplitude and phase, respectively, as:

\[
\sigma_{nA} = V_{FS} \left[ \frac{1}{8} \frac{N}{10^{(SNR_A/10)}} - \frac{2-2b}{12} \right]^{1/2} \tag{6}
\]

\[
\sigma_{n\phi} = V_{FS} \left[ \frac{1}{8} \frac{N\phi}{10^{(SNR_{\phi}/10)}} - \frac{2-2b}{12} \right]^{1/2} \tag{7}
\]

To find the maximum tolerable noise, the amplitude \( A \) in Eqs. (4) and (5) was replaced with \( V_{FS}/2 \), since the maximum SNR must be used to calculate the maximum tolerable noise. A portion of this noise is budgeted for the IA block. It is a good design practice to allocate the majority of the noise budget to the head of the chain (i.e., the IA and the current driver), since the noise of the ADC and ADC driver is divided by the gain of the IA.

C. Analog to Digital Converter

In an EIT system that incorporates a digital matched filter, the ADC is typically located after the instrumentation amplifier, and prior to the matched filter. The ADC’s sampling frequency, resolution, and power consumption are its main characteristics relevant to the EIT SNR. Typically, certain trade-offs are necessary between these characteristics, based on EIT system requirements.

ADCs can be divided into two main categories: Nyquist rate and oversampling data converters. In the bioimpedance and biomedical applications, traditionally delta-sigma [14], [37], [38] and SAR ADCs [8], [39], [40], [41] were employed; whereas the latter is a Nyquist rate ADC, the former is an oversampling data converter. The SAR ADC is generally a medium-speed, medium-resolution converter, while the delta-sigma ADC is a low-speed, high-resolution data converter.

In the following paragraphs, we derive equations and analyze the main circuit performance of the ADC that affects the EIT system specifications.

The resolution of the ADC primarily affects the precision of the EIT measurements. Using (4), the required resolution of the ADC with respect to the amplitude SNR can be written as:

\[
b_A = \frac{1}{2} \log_2 \left[ \frac{1}{12} \frac{V_{FS}^2}{A^2 N_A} - \frac{\sigma_n^2}{\sigma_A^2} \right] \tag{8}
\]

Similarly, the required ADC resolution with respect to the phase SNR using (5) is given by:

\[
b_\phi = \frac{1}{2} \log_2 \left[ \frac{1}{12} \frac{V_{FS}^2}{A^2 \phi^2 N_\phi} - \frac{\sigma_n^2}{\sigma_\phi^2} \right] \tag{9}
\]
Commercial delta-sigma ADCs typically have a resolution around 16 to 24 bits with an effective sampling rate of up to a few hundred kilohertz [42]. SAR ADCs, however, have a resolution between 8 and 12 bits with up to several MHz sampling rate [42]. The SAR ADC is known to have a better figure of merit (FoM), Fig. 6 compares the efficiency of the SAR and delta-sigma ADCs by plotting the FoM versus the effective number of bits (ENOBs) for each type of ADC. This plot includes all Nyquist-rate SAR ADCs and low-pass delta-sigma ADCs that have been published in ISSCC and VLSI [43] since 2008. Note that a few data points for delta-sigma ADCs with FoMs above 1200 fJ/Conv-step are discarded to make the plot more readable. The solid triangle and solid square data points respectively represent the SAR and delta-sigma ADCs implemented in 65 nm technology. This helps us to fairly compare these two ADC structures side by side, since they both use the same technology. To find the average FoM at each ENOB level where the ENOB = b, the mean of the FoMs between b-1 and b+1 is calculated for each of the SAR and delta-sigma ADCs. The solid blue line represents the results for the SAR ADCs and the dashed red line represents the results for the delta-sigma ADCs.

To achieve higher EIT SNR for a given thermal noise ($\sigma_n$), as shown by Eq. (4), one may either reduce the quantization noise by increasing the ADC resolution, or increase the number of the matched filter taps. The number of the matched filter taps may be increased by either increasing the ADC sampling rate or acquiring more samples over multiple periods of the input signal. Here we intend to evaluate whether it is more power efficient to institute a medium-resolution SAR ADC with a higher sampling rate or a higher resolution delta-sigma ADC with a lower sampling rate. As illustrated by the comparison in Fig. 7, one can conclude that in EIT systems it is more power efficient to employ a medium-resolution SAR ADC with a high sampling rate rather than a delta-sigma ADC.

V. INJECTION BLOCK

An EIT system can be implemented by generating a sinusoidal wave (either digitally, or with an analog oscillator), and then injecting the signal into the tissue. In current-mode injection, the injected signal is a current and the resulting voltages that are developed on the surface of the tissue are measured. Alternatively, in voltage-mode EIT systems, a voltage is applied to the tissue, and the induced currents are measured.

The signal generator can be implemented in different ways. Square wave oscillators are one of the simplest designs, in terms of area and circuit complexity, but the odd-harmonic components of the square wave reduce the accuracy of the measurements [45]. Sine wave oscillators provide higher accuracy but are generally more complex. For example, a resistor-chain (RC) DAC based quadrature sinusoid signal generator is presented in [46], where the sine output is taken from chain taps. To have high linearity, many taps and complex DAC designs are required. In [47] a programmable frequency pulse

\[
N = \left(\frac{2}{A^2}\right) \left(\frac{\text{LSB}^2}{12} + \frac{\sigma_n^2}{\text{SNR}}\right) 10^{(\text{SNR}/10)}
\]  
(10)

Let us consider an example scenario, where the target SNR is 80 dB and the thermal noise ($\sigma_n$) is equal to 1 mVrms. Assuming an amplitude of 0.5 V, the number of matched filter taps for different ADC resolutions are calculated using (10), and the results are plotted in Fig. 7. According to the equation for figure of merit of an ADC [44], the power can be written as $P = \text{FoM} \times f_s \times 2^{\text{ENOB}}$. Here, we assume that the input frequency is 10 kHz, and all samples are taken in one period of the input signal. Thus, the sampling frequency of the ADC ($f_s$), is the multiplication of the input frequency (10 kHz in this case) by the required number of taps of the matched filter that was plotted in Fig. 7. The resulting power consumptions by the SAR and delta-sigma ADCs using the mean FoM values for 65 nm technology are plotted in Fig. 8.

As previously stated, to achieve a target SNR, we can either employ a low medium-resolution SAR ADC with a high sampling rate, or a high-resolution delta-sigma ADC with a low sampling rate. As illustrated by the comparison in Fig. 8, one can conclude that in EIT systems it is more power efficient to employ a medium-resolution SAR ADC with a high sampling rate rather than a delta-sigma ADC.
is filtered by a complicated fifth-order switched capacitor low-pass filter to generate a sine wave. A Gm-C oscillator-based analog signal generator is used in [48] to generate sine waves. This structure generally has a limited output frequency and suffers from the inaccuracy of the output frequency. A non-linear-transfer-function-based analog synthesizer [49] converts a non-linear wave such as a triangle wave into a sine wave. This structure suffers from poor linearity.

Modern high-precision EIT systems mostly exploit the advantages that come with digital implementation, including its frequency agility, fast settling, and high frequency resolution. Digital signal processing (DSP) based systems generate sine waves using digitally-stored data points, which require large memory. A pseudo-sine modulation technique is presented in [50] to reduce the memory size, and its variations have been employed in several EIT ASIC systems [15], [40]. The work presented in [63] covers a wide frequency range, up to 2 MHz, using a stepwise signal generator with mixed-time processing to generate a sinusoidal signal. In this work, a discrete-time filter attenuates close-in harmonics, while higher order harmonics are attenuated by a continuous-time filter.

In terms of signal injection, voltage-mode EIT systems using opamps are easier, less costly to design, and have a stable response over a wide frequency span [51]. However, current-mode injection is preferable for the following reasons. Current-mode EIT systems are less sensitive to the errors associated with spatial variations, according to the calculations in [52]. The current-mode approach also provides a better immunity to the unknown skin-electrode impedance, which is a source of error in the voltage-mode scheme [53]. Furthermore, it is easier to control the maximum current passed through tissue in the current-mode approach, which is essential to meet the patient safety requirements [54].

In current-mode EIT systems, the voltage is converted to current prior to application to tissue. Some of the architectures used to achieve this include the modified Howland structure [55], [56], current conveyor based current injection block [57], [58], supply-current sensing current source [59], three-opamp current source [60], and isolated current source using transformer coupling [61]. The ASIC current injection block presented in [8] and [14] use a simple voltage-controlled current source. This structure suffers from high power consumption and low output impedance. Although the ASIC current driver in [62] reports a decent output impedance at a medium frequency range (1 MHz), the authors accounted for parasitic capacitors of packaging and routing in post calculations. However, this cannot be done in a real EIT application; therefore, some parasitic cancellation techniques must be employed.

An EIT system can be constructed using either single-source [63] or multiple-source [64] schemes. In the single-source approach, current is injected (sourced) through one electrode and collected (sunk) through another electrode. In the multiple-source scheme, multiple current sources are employed, while the number of source electrodes is still equal to the sink electrodes, ideally to avoid accumulation of any common-mode voltage in the object under test. Single-source systems are easier to implement. However, the multiplexer that switches the current source between different electrodes adds parasitics, which can degrade the accuracy and frame rate of the system. Use of a multiple-source system reduces the measurement time and parasitics at the price of increased circuit complexity. Multiple current sources in a system need to be very well matched to minimize the common-mode signal [17]. This puts a stringent requirement on the matching and output impedance of current sources in EIT current-mode systems.

In the following we study the main design metrics of the injection block.

A. Noise Budget of the Injection Block

The equations indicating the total amount of noise than can be tolerated in the chain and prior to the matched filter (Eqs. (6) and (7)) were previously studied in the IA section. If we assume that the IA and the ADC driver receive a portion of the total noise budget, the remainder must be allocated for the injection block.

B. Safety Issues and Current Range

In order to have a higher signal-to-noise ratio and better distinguishability, it is desirable to maximize the injected current through tissue. However, concern for the safety of patients restricts the maximum current that can be applied into tissue to avoid ventricular fibrillation and cardiac arrest [65]. According to the standards defined by the International Electrotechnical Commission IEC60601 [66] the patient auxiliary current to be injected through tissue should not exceed 100 µA for frequencies from 0.1 Hz up to 1 kHz, and 10 mA for frequencies above 100 kHz. For the frequency range of 1-100 kHz the amount of the injected current linearly increases with frequency, and can be approximated by 0.1 × f mA, in which f is the frequency in the unit of kHz.
Another safety concern is the skin irritation or burns that may occur due to the applied DC currents to tissue via electrodes. To avoid these problems, DC removal methods can be employed [20], [67].

C. Accuracy

The accuracy of each current source can affect the common-mode voltage, and subsequently the accuracy of the EIT system, as discussed in the IA section. Therefore, here we analyze the accuracy requirements of each current source in single- and multiple-current-source systems.

1) Single source system: In an ideal system with a pair of current sources (one sinking and one sourcing), the sum of the currents equals zero. For each current source, \( \text{LSB}_{CS} \) is defined as the least significant bit equal to \( I_{FS}/2^m \), where \( m \) is the resolution of the current source, and \( I_{FS} \) is the full-scale current. Assuming both current sources have the same accuracy within \( \pm \frac{1}{2} \text{LSB}_{CS} \), the maximum error will be \( \pm \text{LSB}_{CS} \). Therefore, in order to meet the accuracy requirement of the EIT system, the following relationship needs to be met:

\[
\text{LSB}_{CS} < 10^{-\text{Acc}/20} \quad (11)
\]

where in terms of the resolution of the current source we have:

\[
m > \log_2 \left( \frac{I_{FS} \times 10^{\text{Acc}/20}}{\text{LSB}_{CS}} \right) \quad (12)
\]

2) Multiple source system: In a multiple-current-source system with \( C \) (assuming a large number) pairs of current sources (\( C \) sinking and \( C \) sourcing), it is better to look at the problem stochastically rather than as a worst-case scenario. Let us define the standard deviation of current in one unit current source and the total \( C \) pairs of current sources as \( \sigma_o \) and \( \sigma_{oC} \), respectively. Assuming that one unit current source has a \( 3\sigma_o \) equal to \( \pm \frac{1}{2} \text{LSB}_{CS} \), \( 3\sigma_o \) in a multiple current source system with \( C \) pairs of current sources is equal to \( \pm \sqrt{C} \text{LSB}_{CS} \). This shows that the standard deviation of error is increased by a factor of \( \sqrt{C} \) in a multiple current source system. As a result, for a given accuracy, the current sources in a multiple-current-source system must have a more stringent requirement on resolution.

In terms of the common-mode voltage, to meet the same accuracy requirement of the EIT in a multiple-current-source system, the LSB of a unit current source must be \( \frac{1}{\sqrt{C}} \) times the LSB of a unit current source in a single source system. In other words, the resolution of a unit current source in a multiple system, \( m' \), compared to the one in a single source system, \( m \), should follow this relation:

\[
m' = m + \log_2 \left( \frac{\sqrt{C}}{2} \right) \quad (13)
\]

VI. CASE STUDY

In the following, we utilize the knowledge gained in the previous section and incorporate the derived equations to find the optimal design choice. Take as an example an EIT system with 80 dB SNR and 30 frames-per-second as a target. Assume there are thirty electrodes in the system with tetrapolar current injection pattern. This indicates that 435 (= \((30 \times 29)/2\)) patterns need to be applied to acquire one frame.

Referring to (4), infinite permutations of the ADC resolution \( b \), total thermal noise \( \sigma_n \), and the number of samples that the matched filter processes \( N \) are possible to achieve the target SNR. This is shown in the plot in Fig. 9. Here, as an example, we assume that the number of the samples processed in the matched filter is already fixed at 2000 samples \( (N = 2000) \). To meet an 80 dB SNR target, an 8-bit ADC can tolerate up to 2.2 mVrms noise, which can be relaxed to 3.1 mVrms if a 10-bit ADC is utilized instead. Since infinite combinations of \( b, \sigma_n, \) and \( N \) result in the same SNR, we constrain ourselves only to those combinations that minimize the total power consumption.

Selection of the optimal design therefore requires meeting the target SNR and frame rate and minimizing the total power consumption. First, we sweep the values of the ADC resolution and the total noise in (4) to solve for the number of required values that need to be processed in order to achieve the target SNR of 80 dB. The results are shown in Fig. 10(a).

The \( N \) in (4) can be substituted with \( F_s / (FPS \times l) \), where \( F_s \) is the ADC sampling frequency, \( FPS \) is the target frames-per-second, and \( l \) is the number of patterns. In the second step, using the data plotted in Fig. 10(a) and plugging in \( F_s / (FPS \times l) \), the required sampling frequency of the ADC is calculated and plotted in Fig. 10(b).

Now we must solve for the power consumption of the ADC at different sampling frequencies. Therefore, in the third step, we find the FoM of SAR ADCs using data from the ISSCC and VLSI publications for all technologies and ADCs with mega-sample-per-second sampling frequencies, as plotted in Fig. 11.

Using the equation for FoM, the ADC power is defined as \( P = \text{FoM} \times F_s \times 2^{\text{ENOB}} \). In the fourth step, we plug in the values of \( F_s \) and ENOB using Fig 10(b), and the values of the mean FoM using Fig. 11. The calculated ADC power is plotted in Fig. 12.

In the fifth step, we need to calculate the power consumption of the ADC driver. The power consumption of the ADC driver is directly proportional to the resolution of the ADC and hence the size of its capacitive DAC. There are different ways
to implement the DAC block of a SAR ADC. For a $b$-bit SAR ADC with the unit capacitance of $C_u$, the conventional binary-weighted capacitive array has a total capacitance of $2^b \times C_u$, the binary-weighted capacitive array with attenuation capacitor has a total capacitance of $2 \times 2^{b/2} \times C_u$, and the hybrid resistive-capacitive DAC array has a total capacitance of $2^M \times C_u$ (where $M$ is the size of the capacitive portion of the resistive-capacitive DAC). To calculate the power of the ADC driver, we assume a $b$-bit SAR ADC has a total capacitance of $0.25 \times 2^b \times C_u$, with unit capacitance of 20 fF. The dissipation power of the ADC driver is set by the more stringent requirements for the slew-rate and gain bandwidth. Here we assume the power supply of the ADC driver is 3.3 V, and maximum input frequency is 10 MHz. The calculated power consumption of the ADC driver is plotted in Fig. 13.

In the sixth step, we need to calculate the power consumption of the IA to achieve certain input noise levels. Note that the total noise that can be tolerated in the chain is distributed amongst the injection block, the IA and the ADC driver. However, for the sake of simplicity, in our calculations here, we assume that all the noise is generated by the IA. Fig. 14 shows the calculated power of a current-conveyor based IA. Note that to reduce the input referred noise of the IA by ten fold, the IA power consumption needs to be increased by a factor of one hundred. By relaxing the input referred noise of the IA, its power consumption is reduced to the point that the power consumption approaches a constant value. The gain-bandwidth requirement of the IA sets a minimum current (and hence power) that fixes the IA minimum power consumption, regardless of the IA noise level.

In the seventh step, we sum up the power consumptions of the ADC (Fig. 12), ADC driver (Fig. 13) and IA (Fig. 14). The result is shown in Fig. 15.

Fig. 15 shows that, in this design, an input referred noise
of 2 mVrms results in the minimum dissipated power. In the eighth and final step, we select the optimal design considering the available technology. Based on Figs. 15 and 10, the sampling frequency for a 7-, 8-, and 9-bit ADC is 64, 24, and 14 MHz, respectively. In order to select the optimal design choice, one can refer to the database of implemented ADCs, e.g. [43], and look for the ADCs that were implemented in the desired technology. In this way, in a 0.18 μm technology, as an example, a 9-bit ADC with 14 MHz sampling frequency can be selected as the optimal design choice.

Finally, to validate our analysis, we compare predicted to measured signal-to-noise ratio for three different analog front-ends. We applied the performance metrics of the analog front-end circuit components (number of samples, N; ADC resolution, effective number of bits (ENOB); noise) to predict the overall SNR of the EIT system. The result is summarized in Table II.

VII. CONCLUSIONS

In this paper, we studied the main circuit building blocks of a system-on-chip EIT system. Our primary goal was to develop a design methodology that bridges the gap between EIT system-level specifications and circuit-level performance requirements. A related goal was to identify the circuit architectures that best meet the desired circuit-level performance requirements. Among the key findings of this paper are equations and procedures that map the signal-to-noise ratio and the frame rate of the EIT system to the required noise performance of the instrumentation amplifier, the resolution and sample rate of the ADC and the number of matched filter taps, with the objective of minimizing power consumption. Following our proposed design procedure, one interesting conclusion is that low- to medium-resolution SAR ADCs are in general best for meeting EIT specifications, even when high SNR performance is desired. In summary, our paper provides a structured approach for designing high performance, low power ASICs for EIT.

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