An Analog Front End ASIC for Cardiac Electrical Impedance Tomography

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***Abstract*—In this paper an end-to-end CMOS application specific integrated circuit (ASIC) for readout channel in a cardiac electrical impedance tomography (EIT) system is presented. The ASIC consists of an integrated current driver for current injection, an instrumentation amplifier (IA), variable gain amplifier (VGA) at the analog front end for voltage readout from electrodes, and an on-chip 10-bit successive approximation register (SAR) analog to digital converter (ADC) with serial peripheral interface (SPI). The ASIC is fabricated in the CMOS 0.18 μm process with a supply voltage of 3.3 V. Amplitude and phase extraction of the voltages is performed in the digital domain with a matched filter. A fully integrated solution for use in multiple electrode system is demonstrated. The readout chain in the ASIC achieves a minimum signal-to-noise ratio (SNR) of 71 dB over the frequency range of 500 Hz - 700 kHz, while maintaining an average accuracy of 99.7 %. Frame rates of 21 frames per second (fps) for a 32 electrode system is feasible, and the ASIC has an overall power consumption of 11.8 mW.**

***Index Terms*—Electrical impedance tomography, cardiac monitoring, ASIC, current driver, instrumentation amplifier, variable gain amplifier, matched filter.**

I. Introduction

Self-management of chronic heart disease is hindered by three critical barriers: (i) the symptoms that patients monitor today are insensitive, non-specific and late indicators of heart failure [1]; (ii) this lack of predictive strength forces management of the condition to be reactive rather than proactive [2], [3]; (iii) single, once-a-day measurements cannot capture the patient's hemodynamic response to the stresses of daily life activities [4], [5], or the diurnal variation in sympathetic activation [6], [7], thus hindering a full understanding of the patient's condition [8], [9].

One possible solution is to use an implanted device for on-demand telemonitoring of pulmonary artery pressure [10]. Unfortunately, this approach is invasive, expensive, and risks infection, bleeding, arterial embolism, prolonged hospitalization, thrombus and cardiogenic shock, among others [11].

A promising, non-invasive alternative is dynamic electrical impedance tomography (EIT) of the thorax, from which left ventricular volume changes and cardiac output can be extracted. In an EIT system the tissue excitation is performed by injecting alternating current through a pair of electrodes and measuring the boundary voltages induced at the remaining electrodes as shown in Fig. 1. The excitation frequencies can be swept over a pre-determined range depending on the tissue being probed. This idea has been demonstrated previously, including in our own recent work [12] using the EIT Pioneer Set (Swisstom AG, Landquart, Switzerland). The challenge with these systems is that they are large and bulky. They may be appropriate for hospital bedside use, but they are unsuitable for telemonitoring, where physical obtrusiveness and ease of use are critical to ensuring patient adherence [13], [14].

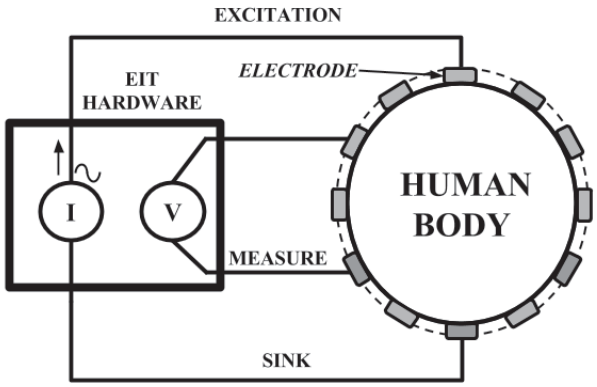

Fig. 1. Block diagram of a typical EIT system. AC current excitation is performed using a pair of electrodes and the voltages induced on the remaining electrodes are measured.

Application specific integrated circuits (ASICs), like the one depicted in Fig. 2, could dramatically miniaturize the cardiac EIT instrumentation system, making its use more feasible in a telemonitoring environment. Unfortunately, the state-of-the-art ASICs for EIT do not meet the performance requirements necessary for cardiac output monitoring. For example, the ASICs described in [15], [16], [17] do not provide adequate signal-to-noise ratio.

In this paper, we present a novel analog front end ASIC that provides the signal-to-noise ratio, interrogation frequency and power consumption performance needed for a cardiac output monitoring application. Section II presents the system level specifications necessary for cardiac monitoring. Section III discusses ASIC building blocks in detail and provides a summary for measured performance. Section IV discusses the system design using the ASIC and provides measured results. Section V summarizes the performance achieved and provides concluding remarks.

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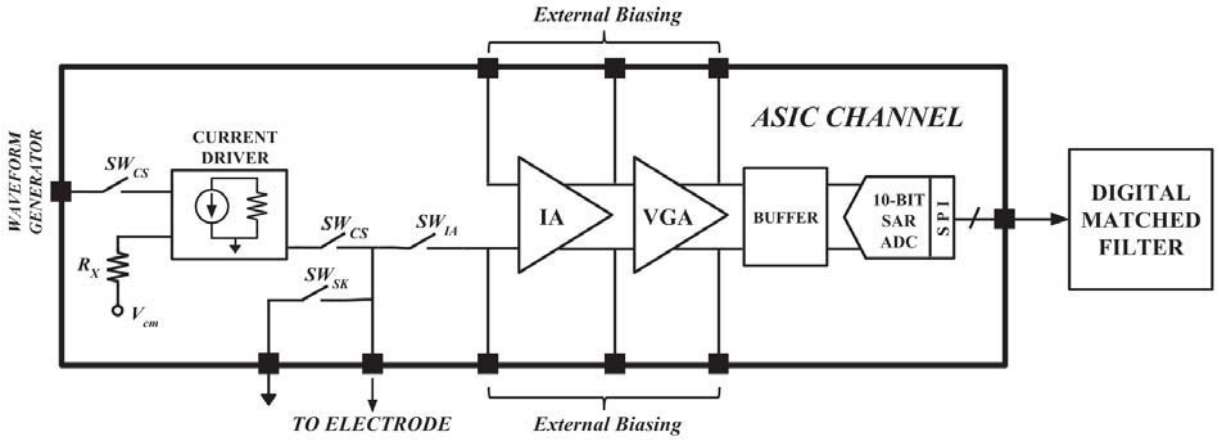


Fig. 2. Block diagram of the cardiac EIT ASIC. The on-chip switches are used to configure the channel in a current-source, current-sink or voltage-read mode. R_X is an on-chip resistor and V_{cm} is the common mode voltage of the current driver. The IA, VGA and the ADC form the voltage readout chain. The digital data from the ADC is sent off-chip using a SPI interface to a digital matched filter for amplitude extraction. Circuit blocks of the ASIC were measured individually with custom built PCBs.

II. EIT SYSTEM LEVEL SPECIFICATIONS

Image reconstruction in dynamic EIT aims to estimate the spatiotemporally-varying electrical properties (conductivity, σ and permittivity, ϵ) within the thorax, provided a set of boundary measurements. These measurements (small-amplitude, imperceptible AC currents that are injected into the thorax, and the resulting voltages that develop on the skin surface), carry information about the internal electrical properties. By solving the inverse problem, it is possible to reconstruct a tomography-like spatial distribution of σ and ϵ.

Over the frequency range 10 Hz to 1 MHz, the conductivity of the blood in the heart is about $\sigma_{\mathrm{h}} = 0.7$ S/m, while that of the background (heart muscle, lungs, fat, bone, etc.) is less than 0.4 S/m [18]. This contrast in electrical properties makes the blood-filled heart visible as a high conductivity region in an EIT image of the thorax. In practice, the frequency of interrogation for cardiac output measurement is at least 20 kHz, in order to avoid the high skin resistivity that would be encountered at lower frequencies [19]. Looking beyond cardiac output measurement, there are some other cardiac EIT applications that might require interrogation frequencies up to 1 MHz. These include bioimpedance spectroscopy for detecting cardiac ischemia [20], measuring fluid index ratio due to edema in congestive heart failure [21], and frequency differencing EIT for anatomic characterization, such as ventricular wall thickness [22]. Also, the entire process of making boundary measurements and constructing an EIT image (a "frame") must be performed at a rate of 14 frames per second (fps) or higher. This way, enough points are captured over the ~ 1 s cardiac cycle such that heart volume change and cardiac output can be calculated.

To understand the remaining performance requirements of a cardiac EIT system, we made use of a highly detailed digital phantom of the human thorax. The phantom comprises the MRI and CT-based 4D XCAT model [23], mesh generation using distmesh [24] and gmsh [25], a perfusion model [26], ex-vivo tissue values of conductivity and permittivity from multiple frequencies [18], and a 3D finite element (FEM) implementation of the complete electrode [27]. We analyzed the digital phantom assuming a 32 electrode EIT system. As shown in Fig. 3, the phantom produces an image that is qualitatively similar to one constructured from measurements of a human volunteer.

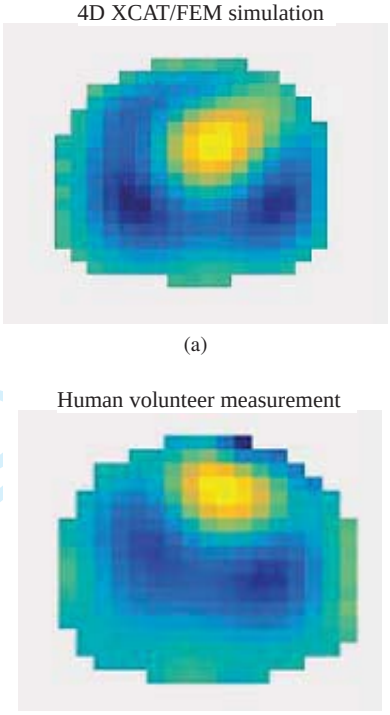


Fig. 3. Cross-sectional conductivity profile of the thorax produced from (a) Digital phantom model; and (b) Bioimpedance boundary voltage measurements of a healthy human subject. The digital phantom model and the in vivo measurements result in qualitatively very similar images, where the heart and lung (from perfusion) are very clearly seen when dynamic EIT imaging is used between end-diastole and end-systole.

Figure 4(a) shows the boundary voltage amplitudes that were generated by the digital phantom for a typical electrode position, with measurements taken at end diastole and also

at end systole. Depending on the anatomy of the subject, the boundary voltages can range in amplitude from tens of millivolts to several hundred millivolts. Interestingly, the voltage measured at end diastole (when the heart is full of blood) is different from that at end systole (just after ejection of blood) by less than 1%. This small change is due to the large amounts of insulating air that are inhaled into the lungs, which confound the relatively smaller signals of blood flow in and out of the heart and cardiac muscle motion.

Since the EIT system must detect the 1% change in voltage amplitude across the systolic cycle in order to extract cardiac output, this would suggest a minimum required signal-to-noise ratio (SNR) of 40 dB. In fact, the EIT image reconstruction problem is poorly conditioned and ill-posed, and demands SNR $>$ 70 dB for this application. Figure 4(b) illustrates how the EIT-derived cardiac output would deviate from ground truth if the SNR fell too low.

In summary, an EIT system for cardiac output monitoring must cover a dynamic range from 20 mV_{pp} to 1 V_{pp}, operate at a frame rate of 14 fps, and maintain an SNR of $>$ 70 dB. In addition, it must support an interrogation frequency of a few tens of kHz, although frequencies up to 1 MHz would be useful for more generalized cardiac EIT applications. Accuracy and linearity requirements are less stringently defined, especially with the use of the calibration techniques that we introduced in [28]. Still, it is typical to design for $\geq 99\%$ accuracy and ≤ -40 dB total harmonic distortion [29], [30], [28].

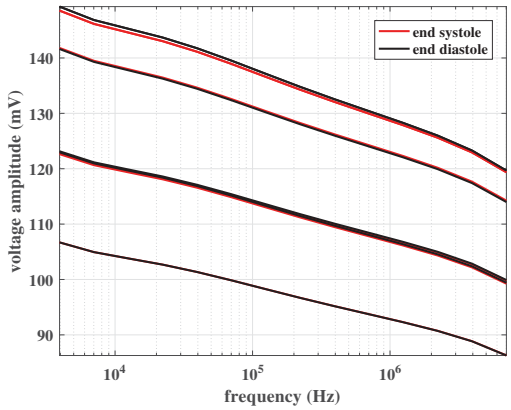
III. ASIC Design and Description

In this section, we describe the different components that comprise the EIT cardiac output analog front end shown in Fig. 2.

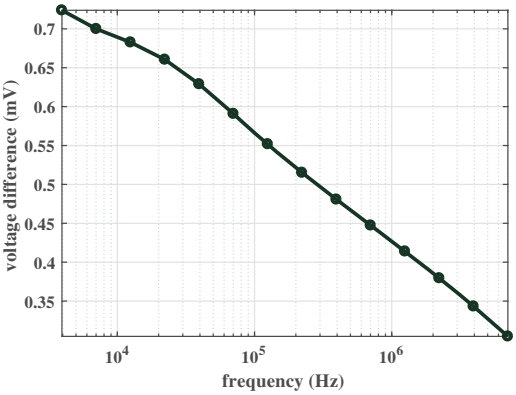
A. Current Driver

System level specifications derived earlier indicate that cardiac monitoring requires an accuracy $\geq 99\%$ and ≤ -40 dB total harmonic distortion. The current driver in the ASIC is capable of generating 1 mA_{pp} sinusoidal current while maintaining total harmonic distortion of $<$ 1 % for frequencies up to 1 MHz. The accuracy of current delivered over this frequency range is $>$ 99.6 %. Accuracy is achieved by designing the current driver with high output impedance, whereas linearity is obtained by using a resistor for voltage to current conversion. The details of the implementation are below.

The current driver for this design is based on the CCII current conveyor [32] shown in Fig. 5. To obtain high linearity, the voltage to current conversion is performed using a 2-stage op-amp in unity gain configuration with a resistor at the terminal X generating current, $I_X = \frac{V_X}{R_X}$ [33]. A class AB buffer at the output of the 2-stage op-amp creates a low impedance node, and the use of indirect compensation technique [34] helps achieve wide-band operation up to 10 MHz. The generated current is mirrored to the output terminal Z through a gain enhanced cascode current structure to provide high output impedance [35], [36], [37].



(a)



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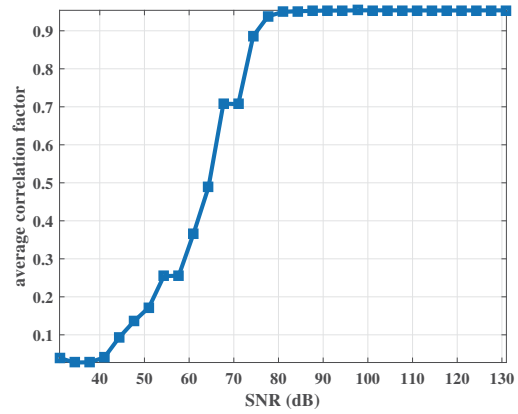

(c)

Fig. 4. (a) Boundary voltage amplitude versus frequency plot for some selected electrodes and current source-sink patterns. (b) The voltage difference between end systole and end diastole measured at the same electrode for a representative source-sink pattern from Fig. 4(a). The difference in voltage at these two time points is less than 1 mV, and decreases with frequency. (c) Effect of measurement SNR on accuracy of the extracted heart area [31]. The y-axis is the correlation factor between actual versus EIT-extracted heart area, averaged across the cardiac cycle. For accurate calculation of cardiac output, the correlation factor should ideally be 1. The plot shows that a measurement SNR of at least 75 dB is necessary for sufficiently-high correlation.

Figure 6 shows an example of the current driver's measurement results. When injecting a 200 kHz, 500 μA_{pp} current onto a 500 Ω load, the measured total harmonic distortion is

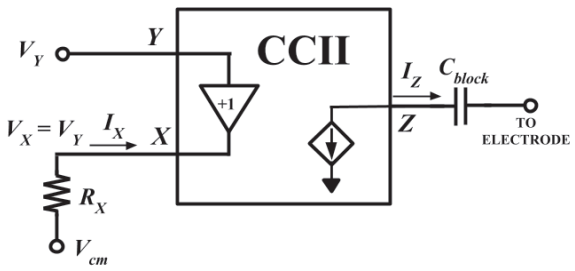

Fig. 5. Block diagram of the current conveyor architecture [32]. Current is generated at terminal X using an on-chip resistor such that $I_X = \frac{V_X}{R_X}$, where $R_X = 500\ \Omega$ and V_X follows the voltage at terminal Y. Current I_X is delivered to terminal Z with a current gain of unity.

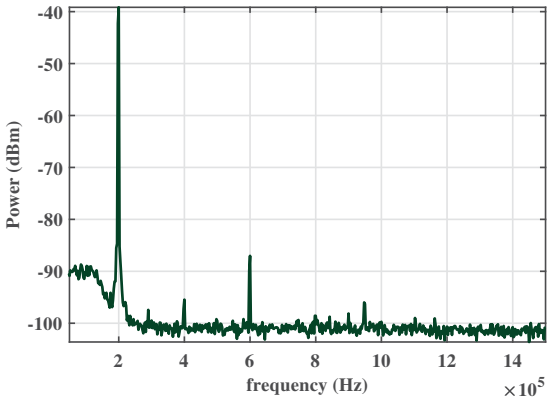

Fig. 6. FFT plot of the current driver delivering 500 μA_{pp} current to a fixed load of 500 Ω. The total harmonic distortion measured is ∼ 0.5 % at an input frequency of 200 kHz.

TABLE I
MEASURED PERFORMANCE OF CURRENT DRIVER.

Parameter	Value
Area	0.26 mm^2
Bandwidth	100 Hz - 10 MHz
Output Impedance	101 kΩ @ 1MHz
Max. Output Current	1 mA_{pp}
THD	$<$ 0.1 % @ 50 kHz
Accuracy	99.6 % up to 1 MHz
Power	1.65 mW

0.5 %. Table I summarizes the other key performance metrics of the current driver.

B. 10-b SAR ADC

The ADC samples the voltage readout chain and provides the digital data to an off-chip matched filter to extract the amplitude and phase. A signal-to-noise ratio of 80 dB is desirable to meet the system SNR specifications. Assuming an output-referred noise of IA, VGA chain of 1 mV_{rms} [38], 80 dB SNR can be achieved with a 10 bit ADC and 100 tap matched filter [39].

Next we discuss the sampling rate of the ADC based on the the desired frame rate of 14 fps. The frame rate is calculated

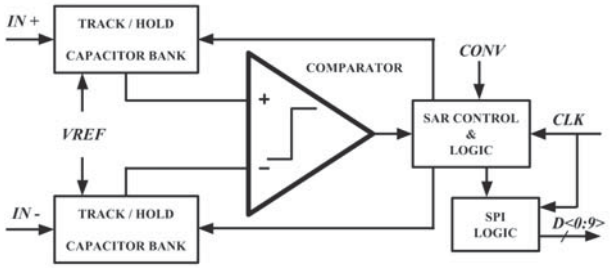

Fig. 7. Block diagram of the differential 10-bit SAR ADC. The maximum sampling rate of the ADC is 250 ksps. Serial data output is achieved by incorporating a SPI interface.

by the following formula,

$$\mathrm{FR} = \frac{1}{\mathrm{P_N} \cdot \left(\frac{\mathrm{N_{tap}}}{f_s} + t_s\right)}\ \text{(fps)} \tag{1}$$

where, FR represents the frame rate in frames per second, N_{tap} is the number of taps in the matched filter for amplitude extraction, P_N is the number of current source-sink patterns in a multi-electrode system, f_s is the sampling rate of the ADC and t_s is the settling time after each pattern is switched. With N_{tap} = 100, P_N = 30 for a 32 electrode system (see discussion on frame rate in section IV), and ideal settling time of zero, the minimum required sampling speed of the ADC is 42 ksps. In reality, the sampling rate should be higher to account for the settling time during pattern switching to obtain desired precision (see discussion on frame rate in section IV). The ADC is designed with a maximum sampling rate of 250 ksps.

An SAR ADC architecture was chosen as it exhibits lower power consumption in comparison to other ADC architectures [40]. The block diagram of the ADC designed is shown in Fig. 7. The track and hold comprises of a capacitor bank and CMOS switches controlled by the SAR logic block. An SPI interface was designed to achieve serial data output which simplifies system level design in terms of input/output infrastructure necessary when the ASIC is incorporated in a multiple electrode EIT system. The 10-bit data is available at the SPI interface after 14 clock cycles when the $CONV$ signal is asserted high. The ADC consumes an average current of 77.23 μA with a sampling rate of 250 ksps and input clock frequency of 3.5 MHz. The dynamic characteristics and measured performance parameters of the 10-bit ADC are shown in Table. II.

The figure of merit for the ADC is given by Eq. 2 [41].

$$\mathrm{FOM_{ADC}} = \frac{\mathrm{P_{avg}}}{f_s \cdot 2^{\mathrm{ENOB}}}\ \text{(J/conv-step)} \tag{2}$$

where, P_{avg} is the average power, f_s is the sampling rate and ENOB represents the effective number of bits for the 10-bit SAR ADC. The ADC achieves an FOM_{ADC} of 1.25 pJ/conv-step.

The FFT plot for a 1 kHz input signal at 250 ksps sampling rate for the ADC is shown in Fig. 8.

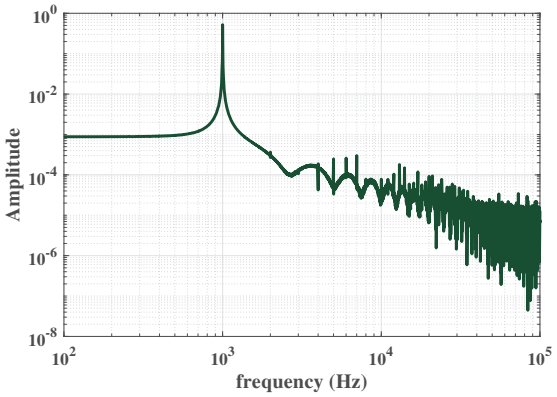

Fig. 8. FFT plot of the ADC for a 1 kHz input signal and sampling rate of 250 ksps.

C. Voltage Sensing Amplifiers (IA and VGA)

Boundary voltages on electrodes for a few selected current source-sink patterns are shown in Fig. 4 (a). The readout chain should amplify these voltages without saturating the channel and provide high linearity (≤ -40 dB) for frequencies up to 1 MHz. The IA is designed with a fixed gain of 3 V/V, as we want to minimize noise, and prevent saturation of the readout chain. The VGA provides three additional gain settings of 1, 3 and 12 V/V. Thus, to amplify the smallest possible voltage (20 mV_{pp}), the readout chain can provide a gain of 36 V/V. The target output-referred noise specification of the IA and VGA chain is 1 mV_{rms}. With a 10-bit ADC and 100 taps in the matched filter, the circuit noise from the voltage sensing amplifiers will provide the required SNR of 80 dB (discussed in the ADC section).

The IA shown in Fig. 9 is a fully differential amplifier based on current conveyors [42]. It has a balanced structure, with high input impedance and linearity. The IA is designed for low noise operation and provides a fixed voltage gain determined by the ratio of two on-chip polysilicon resistors, R_2/R_1. The IA has a common mode rejection ratio (CMRR) over 86 dB, and a measured input-referred noise of 14 $nV_{rms}/\sqrt{Hz}$. The VGA is a fully differential amplifier which has a similar architecture and performance as the IA reported in [38]. Additionally, it has a reconfigurable gain of 0 dB, 9.5 dB and 21.5 dB to fully utilize the input dynamic range of the ADC.

For speed and power constraints, the amplifiers G in Fig. 9 only consists of a few transistors which provide proper level shifting incorporated, for the flipped source follower to increase its dynamic range. It also lowers the output impedance of the source follower, such that the transconductance stage can drive a low value gain resistor R_1 to reduce the overall amplifier noise. The V_{ref} bias voltages are set by on-chip current sources and the implementation of level-shifted source follower concept is similar to our design presented in [38], [43]. The common mode feedback (CMFB) circuit consists of a differential source follower and resistors [44] to control the gate voltage of transistors M_6 and $M_{6'}$.

The magnitude response of cascaded voltage sensing amplifiers which include IA and VGA is shown in Fig. 10. The digitally selectable gains of 9.3, 19 and 30 dB are set by the external control bits. Table. III summarizes the measured performance of the IA and VGA. The measured voltage gains deviate less than $\pm$ 0.5 dB across the 3dB bandwidth. A total of 18 chips were used for this measurement. In addition the variation in gain across the frequencies of the readout chain can be calibrated out for each channel incorporated into the EIT system.

The ASIC is fabricated in the XFAB 0.18 μm CMOS process with a supply voltage of 3.3 V. The micro-photograph of the ASIC is shown in Fig. 11. The current driver, and the readout channel which contains the IA, VGA and the ADC are clearly indicated.

IV. System Design and Results

The system level block diagram of the ASIC channel is shown in Fig. 12. Necessary bias currents and reference voltages needed for the building blocks in the ASIC are provided by using current source IC's and voltage references. The input to the integrated current driver for voltage-to-current conversion is provided with a waveform generator IC, followed by an anti-aliasing filter with a cut-off frequency of 2 MHz. The output current is varied by changing the amplitude of the sinusoidal input voltage to the current driver. To sense the accurate current injected into the electrode, external sense resistors with switching mechanism is designed on the board. External ADC with anti-aliasing filter is also included as a backup. The output from the on-chip ADC and external ADC's is interfaced to a field programmable gate array (FPGA) using SPI communication protocol. The board is powered with linear dropout regulator (LDO) IC's which provide two voltage levels of 1.8 V and 3.3 V.

TABLE II
Measured performance of 10-bit SAR ADC.

Symbol	Parameter	Value
V_{DD}	Process 0.18 μm	1.8 V
V_{IN}	Differential Input Voltage	0 - 1.2 V
F_s(max)	Sampling Rate	250 ksps
SINAD	Signal to Noise and Distortion	54.98 dB (1 kHz)
ENOB	Effective number of bits	8.84
P_{avg}	Average Power	139 μW
FOM_{ADC}	Figure of Merit	1.25 pJ/conv-step

TABLE III
Measured IA and VGA Performance Summary

	IA	VGA
V_{DD}	3.3 V	3.3 V
Power	2.07 mW	4.66 mW
Bandwidth	>10 MHz	>10 MHz
Input Impedance (DC)	>1 GΩ	>1 GΩ
Input Noise ($nV_{rms}/\sqrt{Hz}$)	14	80 / 27 / 6.7
Gain (dB)	9.3 (1 kHz)	0 / 9.3 / 21 (1 kHz)
THD (dB) ($V_{out,diff} = 2V$)	-63 (1 kHz)	-70 (1 kHz, A_v = 21 dB)

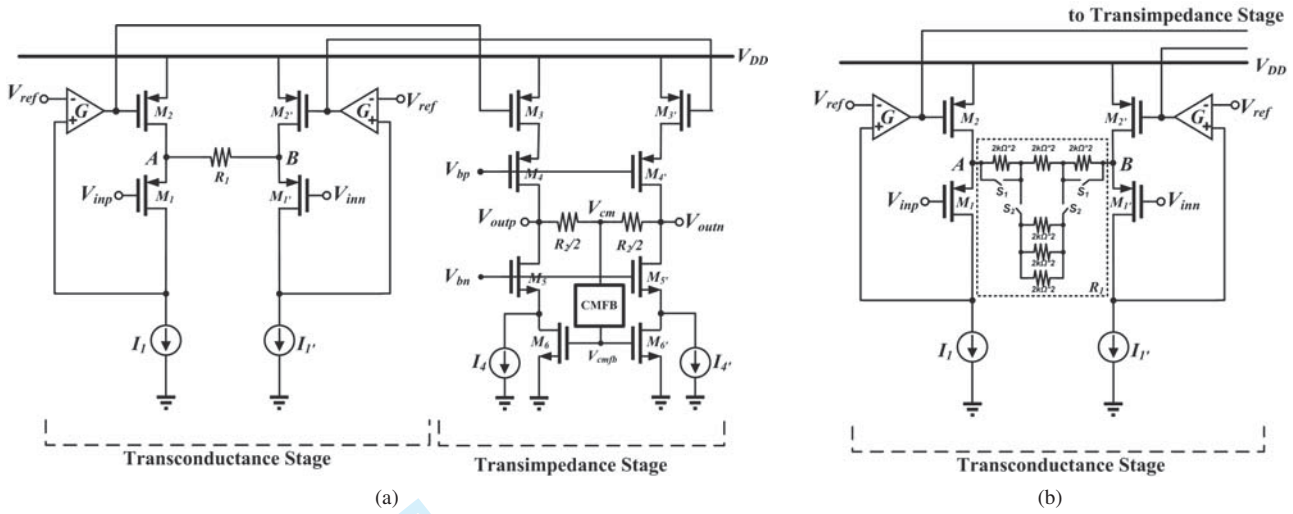

Fig. 9. (a). Simplified schematic of the current conveyor architecture used to implement the IA. The fixed gain is determined by the ratio of on-chip polysilicon resistors $R_1 = 10$ kΩ and $R_2 = 30$ kΩ. (b). The transconductance stage of the VGA is shown, while the transimpedance stage has a similar structure as the IA. Variable gains for the VGA is achieved by the on-chip resistor ladder shown in the figure. Resistor $R_2 = 15$ kΩ in the transimpedance stage is fixed while resistor R_1 in the transconductance stage is variable with values 15 kΩ, 5 kΩ and 2.5 kΩ. Digital control of variable gains is achieved using switches S_1 and S_2.

A. System Signal-to-Noise Ratio (SNR)

The SNR of the system indicates the noise in the readout signal chain of the EIT system. According to our analysis, the acceptable SNR for accurate cardiac output monitoring should be ≥ 70 dB. The SNR formula is given by [28].

$$\text{SNR} = 10 \cdot \log_{10} \cdot \left\{ \frac{\sum_{n=1}^{N} V_n^2}{\sum_{n=1}^{N} (V_n - \overline{V})^2} \right\} \quad (3)$$

where N is the repeated number of SNR measurements, V_n represents the measured SNR value of the signal chain, and $\overline{V}$ represents the mean of all measurements. The ASIC was configured in the voltage readout mode, and the readout channel gain settings chosen such that the ADC input dynamic range was utilized. The ADC sampling rate was set at 250 ksps and the input frequencies swept from 500 Hz to 1 MHz. The digital data from the ADC was sent off-chip and a matched filter used to extract the amplitude. To obtain the SNR of the readout signal chain, $N = 128$, repeated number of measurements were performed. The minimum SNR measured is 71 dB over a frequency range of 500 Hz - 700 kHz. At frequencies > 700 kHz the input amplitude had to be reduced to prevent distortion and accounts for the drop in SNR value. The measured SNR plot over frequencies of 500 Hz to 1 MHz is shown in Fig. 13.

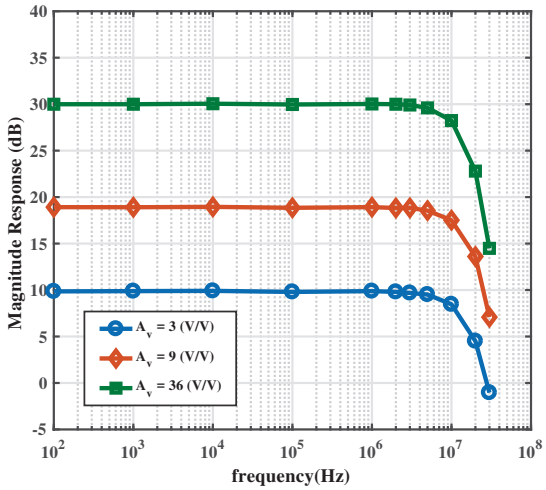

Fig. 10. Measured magnitude response of the readout channel (IA and VGA cascaded). The IA provides a fixed gain of 9.3 dB, whereas the VGA can be programmed to achieve a gain of 0, 9.3 and 21.5 dB with external control bits.

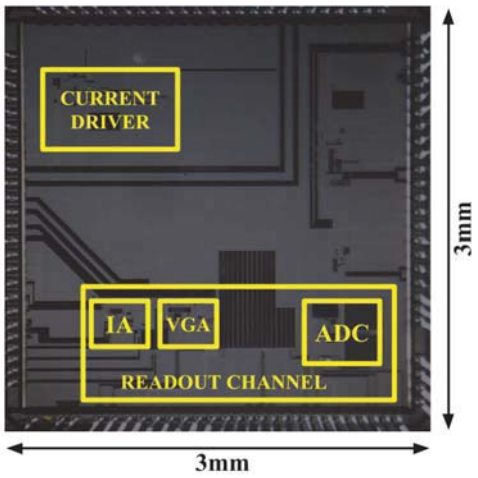

Fig. 11. Chip Micro-photograph. The current driver and the readout channel are shown.

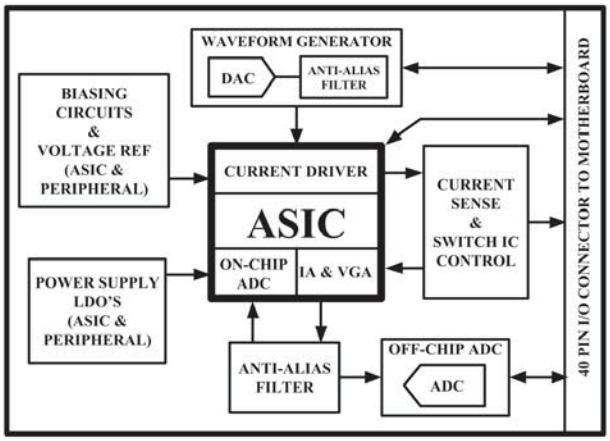

Fig. 12. Block Diagram of the PCB module. The core ASIC is shown with additional circuitry for power supply, biasing, waveform generation, current sensing, switch control, off-chip ADC, and anti-aliasing filters. The 40 pin I/O headers mounts onto a motherboard PCB and contain a large number of ground pins for signal integrity.

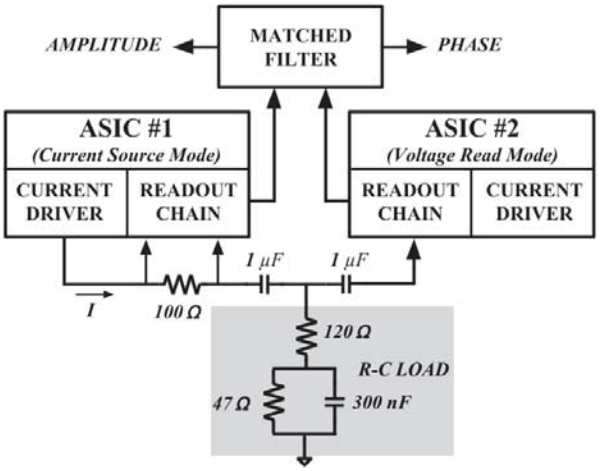

Fig. 14. Setup for obtaining Cole-Cole plot. Representative R-C load is selected via 4D XCAT simulations. Measurement is performed by two channels of the ASIC. Amplitude and phase extraction is performed in the digital domain with a matched filter. Calibration is incorporated to obtain accurate measurements.

B. Cole-Cole Plot

An R-C circuit combination is used to model the complex tissue impedance of the thorax. The representative load is chosen from simulations using the 4D XCAT model described earlier, where the voltages induced on the electrodes from select current injection patterns are analyzed across frequencies, (see Fig. 4 (a)). The block diagram for the measurement of the representative complex impedance is shown in Fig. 14 which incorporates two ASIC channels. One channel is configured in the current source mode and the accurate current injected in to the R-C load is determined by measuring the voltage across the 100 Ω sense resistor. The second ASIC channel is configured in voltage read mode and measures the voltage induced on the R-C load circuit due to the injected current. In order to obtain high accuracy, a calibration method is adopted where a known value of current (500 μA) is injected into a fixed resistance (200 Ω). The R-C circuit components, sense resistor and associated parasitics are measured using a LCR meter. To ascertain the exact gain of the readout channel, gain values are incorporated from the measured results of the IA, VGA specifications over frequencies of interest. This data is saved as reference for actual measurement of load and used for calibration. The measured Cole-Cole plot for frequencies of 250 Hz - 1 MHz is shown in Fig. 15. An average of 50 measurements are performed for each frequency point and the amplitude and phase are extracted using a matched filter.

Cardiac EIT systems typically have accuracies $>$ 99 % as it is necessary to measure small impedance changes. The accuracy of the ASIC readout chain is calculated using Eq. 4.

$$\text{Accuracy } (\%) = \left(1 - \frac{V_{meas} - V_{sim}}{V_{sim}}\right) \cdot 100 \qquad (4)$$

where V_{meas} is the measured voltage and V_{sim} is the voltage obtained from theory. The measured amplitude accuracy and phase error over frequencies is plotted in Fig. 16. An average accuracy of 99.7 % is obtained for the measurement of complex impedance amplitude.

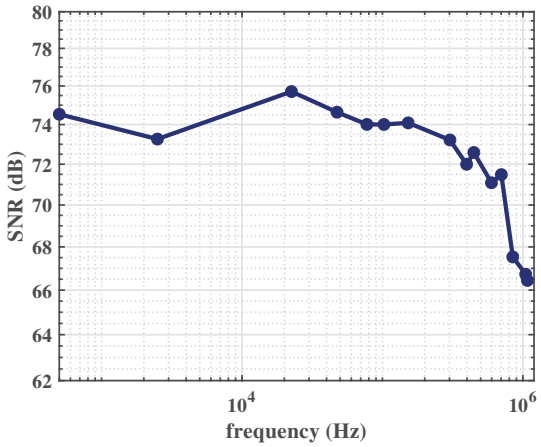

Fig. 13. Signal-to-noise ratio (SNR) at the output of the matched filter that follows the ASIC. SNR was measured using Eq. 3.

C. Frame Rate

To detect the change of heart volume and for accurate cardiac output monitoring the frame rate should exceed 14 fps as shown in our discussion earlier. The frame rate for the system is calculated by Eq. 1. It is typical in Swisstom systems and EIDORS modeling [45] to utilize skip patterns for single-ended voltage measurements. In a 32 electrode system using skip patterns, $P_N = 30$. The settling behavior after pattern switching can be studied with the help of the circuit used for measuring the complex impedance shown in Fig. 14. The RC time constant is determined by the DC blocking capacitor (1 μF) and the resistive load (167 Ω). To achieve a 10 bit resolution the voltage at the load requires 7 time constants [46] to settle. N_{tap} is set to 100 and the ADC is sampled at 250 ksps. Frame rates of $\sim$ 21 fps is feasible with the designed ASIC.

TABLE IV
PERFORMANCE COMPARISON OF ASIC'S FOR ELECTRICAL IMPEDANCE TOMOGRAPHY

Reference	[15]	[16]	[17]	This Work
Process	0.18 μm CMOS	0.18 μm CMOS	65 nm Mixed CMOS	0.18 μm CMOS
Frequency	up to 90 kHz	10 - 200 kHz	10 - 256 kHz	500 Hz - 700 kHz
Current Injection (peak-peak)	100 - 350 μA	0.1 - 1 mA	0.1 - 1 mA	up to 1 mA
Voltage Gain of Readout Chain (dB)	18 - 40	18 - 60 (6 dB step)	20 - 70 (6 dB step)	9.3, 19, 30
ADC (Sampling Rate)	10-bit (N/A)	10-bit (1 - 200 ksps)	10-bit (1 - 256 ksps)	10-bit (12.5 ksps - 250 ksps)
SNR (dB)	40	56.3[1]	N/A[2]	71[3]
Power (mW)	6.3	1.733	6.69	11.8[4]
FOM (pW/Hz)	700	13.27	N/A	4.75

[1] SNR averaged over measurement index [16].
[2] SNR was not reported. However, the analog matched filter approach used in [17] typically provides an SNR of less than 60 dB.
[3] The minimum achieved SNR is 71 dB over frequency range of 500 Hz - 700 kHz, whereas for the frequency range of 500 Hz - 1 MHz, the minimum achieved SNR is 66.7 dB.
[4] Breakdown of power is as follows. The current driver consumes 1.65 mW, IA and VGA consume 6.73 mW, and the ADC and its driver consume 3.44 mW.

D. Comparison

Table. IV summarizes the performance of this work with previously reported literature on EIT ASIC's. A figure of merit for the ASIC channel is defined by Eq. 5 [47],

$$\text{FOM} = \frac{\text{Power}}{\text{BW} \cdot 10^{\left(\frac{\text{SNR}}{20}\right)}} \ (\text{W/Hz}) \qquad (5)$$

where, Power is the average power consumption per ASIC channel, BW is the bandwidth of the system, and SNR is the minimum signal to noise ratio in decibels over frequency range of 500 Hz - 700 kHz. As seen in Table. IV the ASIC used for cardiac output measurements in this work is more power efficient than other designs with the lowest FOM of 4.75 pW/Hz. This is achieved by designing an IA and a VGA with wider swing, lower noise and high linearity [38], [43].

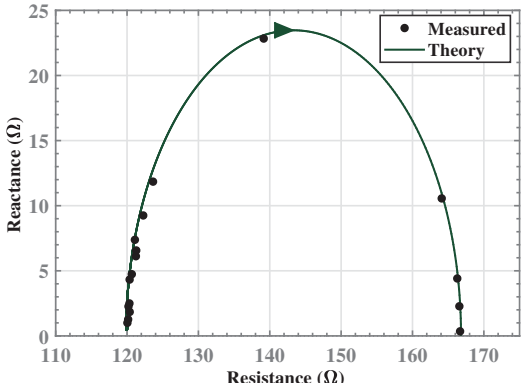

Fig. 15. Cole-Cole plot for a parallel RC load shown in Fig. 14. The measured results are compared with theory for frequencies from 250 Hz - 1 MHz.

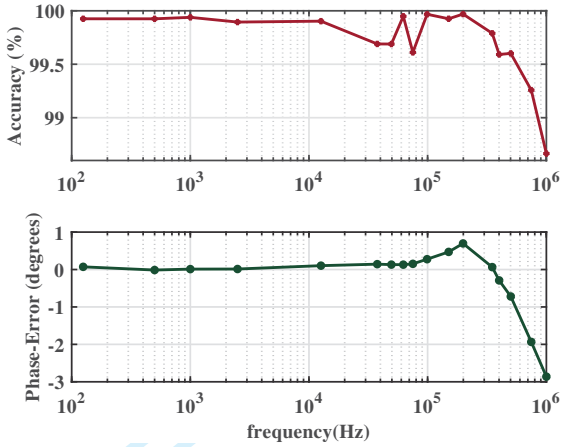

Fig. 16. Accuracy of measured amplitude and phase error over frequencies.

V. CONCLUSION

The cardiac EIT system consists of several components such as the analog front-end for signal processing, the digital domain for single point impedance computation, FPGA block for control and communication strategies and reconstruction software to obtain the final image of the thorax. Some of the challenges associated are the signal processing on the ASIC up to 1 MHz, control strategies for electrode switching using FPGA, and robust board design for maintaining signal integrity. This paper measures the performance of the analog chain alone, without it being confounded by other components of the EIT system.

An ASIC with all analog front end components of a cardiac EIT system is fabricated in the CMOS 0.18 μm technology and individual blocks are characterized. The integrated current driver delivers currents up to 1 mA_{pp} while maintaining a THD of < 1 %. The voltage sensing amplifiers provide gains of 9.3, 19 and 30 dB to process the dynamic range of voltages

incident on the electrodes. The readout chain in the ASIC achieves a minimum SNR of 71 dB over frequency range of 500 Hz - 700 kHz at the output of the matched filter. An average accuracy of 99.7 % is measured by incorporating a representative R-C circuit and calibration scheme. Frame rates of 21 fps are feasible for a 32 electrode system for single ended measurements. The use of power efficient SAR ADC with serial interface for data acquisition enables the ASIC to be used in a multiple electrode EIT system for cardiac output monitoring. The ASIC achieves the desired SNR, frame rate and accuracy specifications with a power consumption of 11.8 mW.

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