A Power Adaptive Variable Gain Instrumentation Amplifier for Electrical Impedance Tomography

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***Abstract*—In this paper, we present an instrumentation amplifier for electrical impedance tomography. The instrumentation amplifier is designed to process a wide dynamic range input, based on a fast automatic gain control technique that minimizes measurement latency. In addition, the instrumentation amplifier employs a reconfigurable power scheme that allows it to adjust its total power consumption depending on the frequency of the input signal as well as on the phase of the measurement cycle. Results from a 3.3 V, 180 nm CMOS process simulation show that the proposed instrumentation amplifier can process signals up to 6 MHz, with an amplitude of 2 V_{pp}. The instrumentation amplifier maintains an SNR > 50 dB down to input amplitudes of 1.07 mV, and it has an average power consumption of 698 μW (< 500 kHz operation) and 5.97 mW (> 500 kHz operation).**

I. Introduction

Electrical impedance tomography (EIT) is a promising low-cost technology for biomedical imaging. Translating this technology to the clinic may require the integration and miniaturization of the electronics that are used to measure tissue electrical properties. Towards this end, we are designing an integrated circuit instrumentation amplifier (i-amp) for high-frequency EIT applications.

Unlike recent designs like [1] and [2], the i-amp for our target applications must process input signals over a wide dynamic range (up to a 2 V_{pp} input signal, and a noise floor as low as 100 μVrms) [3]. To meet the dynamic range requirement, the typical solution is to use automatic gain control (AGC)[2]. Unfortunately, conventional AGC increases the latency of the i-amp, resulting in low frame rate, which in turn reduces the imaging quality and the temporal resolution of the system.

To improve imaging contrast, the EIT system (and i-amp) must operate at frequencies from 100 Hz to several MHz. Simply increasing the power consumption of a state-of-the art biopotential i-amp, like that of [4], is not a viable option for achieving high frequency operation. This is because an excessive amount of power dissipation would impede the ultimate goal of designing a miniaturized system.

We recently introduced an i-amp architecture with AGC that produces minimal latency, thus achieving wide dynamic range operation while maintaining the system's frame rate. The circuit that we presented was unfortunately susceptible to device mismatch, which would degrade its common mode rejection performance, as well as the AGC's efficacy. In addition, our previous circuit consumed a large, fixed amount of power in order to accommodate 10 MHz input signals.

In this paper, we present implementation details and simulation results of a new i-amp – based on the architecture of [5] – that is robust to device mismatch, and also achieves a lower average power consumption.

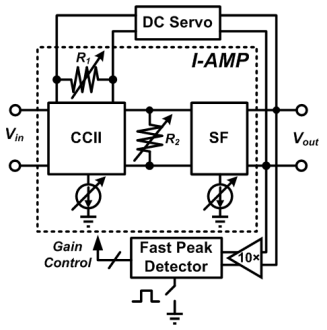

Fig. 1. Instrumentation amplifier architecture. The core of i-amp consists of the CCII, the source follower and variable resistor R_1, R_2. The CCII and R_1, R_2 form the transconductance stage and the transimpedance stage, the source follower acts as an output stage. The resistance values of $R_1$and R_2 depends on the output of the fast peak detector.

II. System Overview

Figure 1 shows the block level diagram of our proposed system. It is based on a universal current conveyor instrumentation amplifier core [6], which allows for easy gain control, and has an inherently high common mode rejection ratio (CMRR) [6]. The fast peak detection circuit provides low-latency automatic gain control.

To reduce the effect of transistor mismatch in the i-amp core – this is the limiting factor for CMRR –, a continuous-time DC servo-loop [7] is used to steer counterbalancing currents into different internal branches of the i-amp. Transistor mismatch also reduces the resolution of the peak detector circuit, but this resolution problem can be overcome with a $10\times$ gain block at the input of the peak detector. In practice, we implement the $10\times$ gain by initializing the i-amp gain to 20 dB at the start of every measurement cycle.

For power efficiency, the bias currents of the i-amp core are programmable to either a 'high' or 'low' setting, depending on the input signal frequency. Also, portions of the peak detection circuitry are disconnected from the power supply

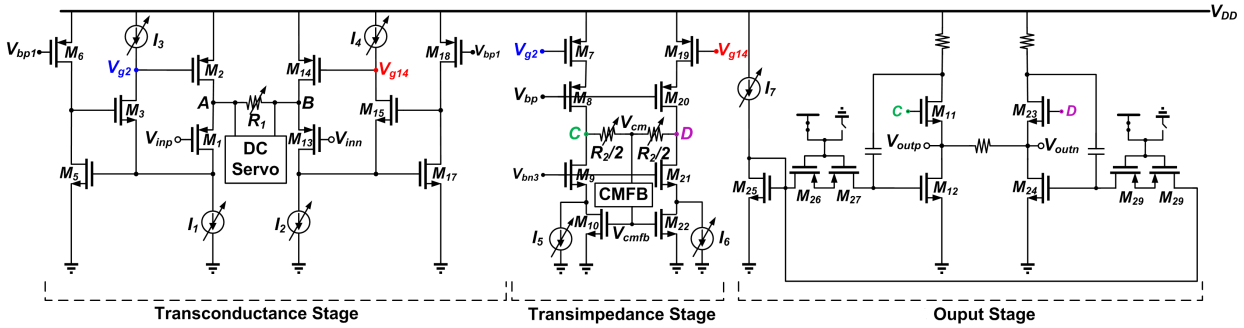

Fig. 2. Circuit diagram of the instrumentation amplifier core. Both resistance of $R_1$and R_2 depend on the output code of the fast peak detector. The equivalent load capacitance at node V_{outp},V_{outn} from the ADC driver is 1.5pF, which are included in all simulations.

for the majority of the time; they are powered on only at the beginning of each measurement cycle, when the gain control setting is being calculated.

III. Instrumentation Amplifier Core

The instrumentation amplifier core consists of a transconductance stage, a transimpedance stage and an output stage (Fig. 2). The transconductance stage converts the input AC voltage, $V_{\rm in} = V_{\rm inp} - V_{\rm inn}$, into a current $V_{\rm in}/R_1$. This current is transmitted to the transimpedance stage, which produces a voltage across R_2: $V_{\rm CD} = V_{\rm in} \times R_2/R_1$. So, the gain of the i-amp is R_2/R_1 . The output stage is a low power class AB buffer [8], and it is used to drive a 1.5 pF load capacitance.

A. Transconductance stage current conveyor

The current conveyor in the transconductance stage uses a pair of flipped voltage followers (M_1, M_{13}) to buffer the input signal from nodes $V_{\rm inp,n}$ to nodes A and B. Simple common drain voltage followers are unsuitable for this task, as their source currents would be input-dependent (due to resistor R_1), resulting in degraded linearity.

To further improve the linearity of the flipped followers, the voltage drops across I_1 and I_2 are pinned to the V_{gs} of transistors M_5 and M_{17}, respectively. This improves linearity in a number of ways. First, it minimizes the effect of channel length modulation in I_1 and I_2, thus keeping the followers' bias currents constant. Also, it shields the drain voltages of M_1, M_{13} from changes in V_{g2}, V_{g14}, which allows M_1, M_{13} to remain in saturation for large input voltage swings. Finally, the common source amplifiers M_5 (M_{17}) and M_3 (M_{15}) effectively reduce the source node impedance of transistor $M_1(M_{13})$ by a factor of $(g_{\rm m}r_{\rm o})^2$. This allows M_1 and M_{13} to maintain their source follower functionality even when driving the low values of R_1 that are necessary for high frequency operation [5].

B. Variable Resistors

R_1 and R_2 are each implemented as a network of switches and resistors (Fig.3 (a)) based on a unit-sized unsilicided poly resistor. R_1 and R_2 can be programmed to different resistance values, depending on the amplitude and frequency of the input signal (Table I).

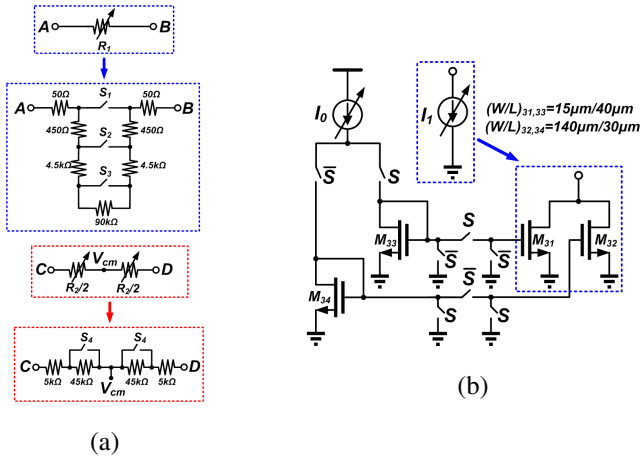

Fig. 3. (a) Simplified schematic of variable resistors R_1 and R_2. (b) For the i-amp's low frequency setting, I_0 is set to 22μA, the S switches are closed and the $\bar{S}$ switches are open. This way, the I_1 current source in the transconductance stage of Fig. 2 is implemented by the current mirror formed by M_{31} and M_{33}. The small W/L ratio of $M_{31,\,33}$ ensures that it is in above threshold, with a low transconductance. Similarly, the M_{32}, M_{34} current mirror implements the I_1 current source when the i-amp is in its high frequency setting. The large W/L ratio of $M_{32,\,34}$ ensures that its gate overdrive voltage is small enough that it remains in saturation.

The i-amp gain, R_2/R_1, is programmed to be 100 for input signal amplitudes less than 20 mV_{pp}. For amplitudes between $20mV_{pp}$ and $200mV_{pp}$, the R_2/R_1 ratio is 10, and for larger signals, the ratio is 1. At a given frequency of operation, these different ratios are achieved by holding R_2 fixed and then varying R_1 accordingly. Since R_1 contributes the majority of the i-amp noise, varying R_1 has the effect of maintaining a constant output-referred noise, regardless of gain setting. This also means that the signal-to-noise ratio (SNR) at the i-amp

TABLE I
Variable resistors R_2, $R_1$for the different gain/bandwidth settings.

	R_2/R_1	
	BW$\leq$ 500 kHz	BW$>$ 500 kHz
G=1	100kΩ/100kΩ	10kΩ/10kΩ
G=10	100kΩ/10kΩ	10kΩ/1kΩ
G=100	100kΩ/1kΩ	10kΩ/100Ω

output remains constant.

The bandwidth of the i-amp is largely determined by R_2 and the load capacitance on its terminals. To accommodate high frequency input signals, the i-amp bandwidth is set appropriately high by programming R_2 to 10kΩ. For lower frequency ($\leq$ 500 kHz) signals, R_2 is programmed to 100kΩ, and R_1 is also increased accordingly. These larger resistor values require less current to flow through them in order to generate the same voltage swings as before. Hence, the bias current levels I_1-I_7 can be reduced when the i-amp is in its low bandwidth setting.

C. Variable Bias Currents

The bias currents sources I_1-I_7 are implemented as transistors operating in saturation. By adjusting their gate voltages, these transistors are programmed to produce different levels of bias currents depending on the input signal frequency (see Table II). Because of the wide variation in current levels for the different frequency settings, there are a number of design implications that must be considered.

The DC bias voltages of nodes A and B are chosen carefully so that the M_1, M_{13} voltage followers are always in saturation, even when processing a 2 V_{pp} input signal. Now, depending on the i-amp frequency setting, the source current of M_1, M_{13} is either 25μA or 255μA. To prevent the DC voltages of nodes A and B from changing significantly in response to these different current levels, we size M_1, M_{13} at $W/L = 640\mu m/300nm$, ensuring that they operate deep in subthreshold.

For low noise operation, it is desirable to make the transconductance (g_m) of transistors M_1, M_{13} much larger than that of any other transistors. This is particularly true for the transistors that form the I_1, I_2 current sources; they begin to contribute significantly to the i-amp noise if their g_m values are similar to that of M_1, M_{13}. Using a fixed, small W/L ratio for the I_1, I_2 transistors is inadequate, because this would push them out of saturation for the high current setting. Instead, we switch in different-sized transistors (see Fig. 3) for I_1, I_2, for each bias current level. This way, the I_1, I_2 transistors always have relatively small g_m (good for noise), and they always remain in saturation (good for linearity).

In our previous design [5], we used passive common mode feedback (CMFB) to set the common mode levels of nodes C and D. In this design, since we are varying the currents of I_5, I_6, a passive CMFB scheme would shift the DC points of nodes C and D, causing a reduction in output voltage swing. To resolve this problem, we use an amplifier-based CMFB, which keeps the common mode level of nodes C and D fixed, independent of the values of I_5, I_6.

TABLE II
BIAS CURRENT LEVELS FOR THE DIFFERENT BANDWIDTH SETTINGS.

	BW$\leq$ 500 kHz	BW$>$ 500 kHz
$I_{1,2}$	22μA	275μA
$I_{3,4}$	15μA	240μA
$I_{5,6}$	2μA	25μA
I_7	5μA	25μA

IV. Fast Peak Detector

Each voltage measurement should ideally take only 1 period, in order to have the highest frame rate possible. Unfortunately, automatic gain control involves peak detection, which adds some latency to the measurement time. So, to minimize the loss in frame rate, it is important to have a peak detector that converges to the correct gain setting within a small fraction of a period.

Our proposed fast peak detector works by shifting the input signal by 90 degrees, and then summing up the squares of the two phase-shifted signals. The result of this summation is the square of the input signal's amplitude [5], which is converted into a 2-bit gain control code.

V. Results

We designed the adaptive-power variable gain instrumentation amplifier in a 3.3 V, 180 nm CMOS process. The current consumption of the i-amp core is adjustable at 154μA and 1.25mA, while the biasing circuits consume 52μA and 555μA.

Figure 4 shows the magnitude response plots of the i-amp. For the high current setting, the gain is alterable at 39, 20 and 0.49 dB (39, 19.6 and -0.11 dB for the low current setting), the i-amp maintains its gain within $\pm$0.5 dB variations up to 26, 21 and 6.8 MHz (1.73, 5.65 and 0.78 MHz for the low current setting). The phase response in Fig.5 shows for gain of 1, 10, 100 (V/V), the i-amp maintains phase variation within $\pm 1^\circ$ till 0.47, 1.72 and 0.51 MHz for the high current setting and 37, 593 and 125 kHz for the low current setting. Figure 4 and 5 show peaking in low gain settings. This peaking could possibly be a result of low frequency zeros ($-g_{m,in}/C_{gs,in}$) that are created by the large-sized input transistors.

Figure 6 shows the i-amp's output referred noise voltage noise density versus frequency for different gain and current settings. The total output noise (integrated from 0.01 Hz to 1 GHz) is dominated by the input transistor and the variable resistor R_1. For the same gain setup, the total integrated noise at the low current setting is nearly twice that of the high current setting because the total parasitic capacitance associated with node C, D (see Fig.2) is decreased by a factor of two.

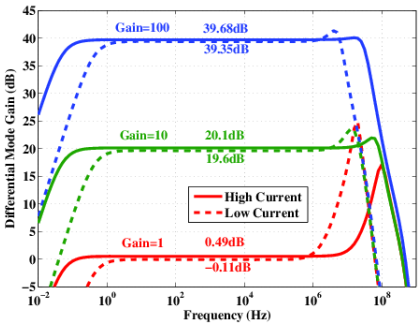

Fig. 4. Magnitude frequency response of the i-amp.

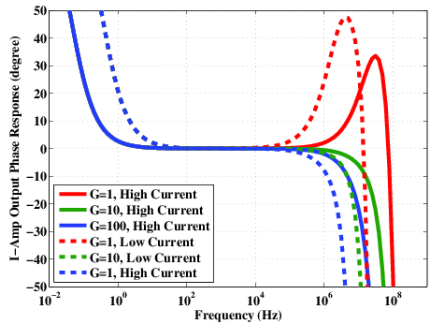

Fig. 5. Phase response of the i-amp.

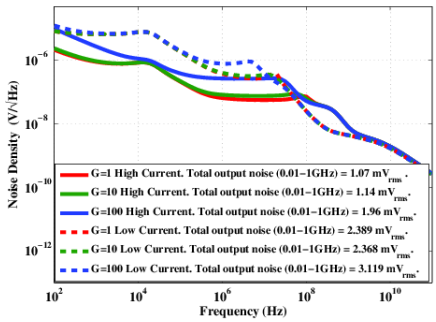

Fig. 6. I-amp output voltage noise density and total integrated noise.

Figure 7 shows the power saving and fast settling behaviors of the peak detector unit. The power supply is turned on for 18μs at a time. This accounts for a 15μs start up time, 2μs to perform the squaring and summing operation, and 1μs to latch the digital gain control code at the peak detector's output.

Monte Carlo simulations based on foundry-provided test data and models are used to estimate the i-amp's CMRR performance. Table III summarized i-amp's average CMRR under different conditions, it shows the DC servo loop improve the average CMRR at high input frequencies.

VI. Conclusions

We have presented an instrumentation amplifier for an EIT system that can process a high dynamic range input up to 2 V_{pp} over a 6 MHz frequency range. The instrumentation amplifier uses a fast peak detector to minimize measurement

TABLE III
SIMULATED I-AMP CMRR - MEAN (σ)
(MONTE CARLO SIMULATION: 3σ, 2000 RUNS FOR EACH SETUP)

$Freq_{in}$	100kHz				1MHz		5MHz	
Servo	Yes		No		Yes	No	Yes	No
Current	High	Low	High	Low	High		High	
G=1	87.2 (7)	72.7 (6.5)	90.2 (6.1)	72.6 (7.8)	76.4 (6)	74.4 (6)	64.8 (6)	58.5 (6.7)
G=10	96.9 (7.6)	89.9 (5.4)	96.4 (7.2)	89.2 (5.8)	91.7 (5.3)	88.1 (6.3)	82.9 (5.8)	74.7 (7.3)
G=100	94.5 (9.4)	95.9 (6.5)	93.5 (7.5)	94.5 (6.7)	93.5 (7.3)	86.6 (6.9)	91 (7.2)	75 (8.1)

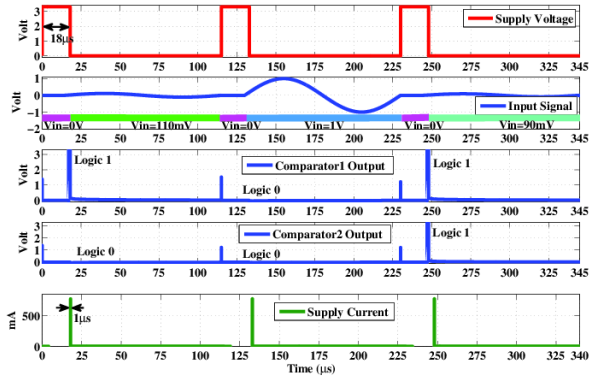

Fig. 7. Fast settling of the peak detection block. Input signal consists of three single period 10 kHz signals with no signal between each period (15μs). The supply voltage is on for 18μs each time, beginning 15μs before each input signal period. The peak detection process takes 3μs (3% of the input period). Comparator outputs shows digital bits for gain of 10, 1, 100 (V/V) corresponding to V_{in}=110 mV, 1 V, 90 mV. Duration of comparator results is long enough for digital logic block to process and pass control bits to the i-amp core.

latency and it is able to adjust its total power consumption according to the frequency of the input signal.

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References

[1] A. Worapishet, A. Demosthenous, and X. Liu, "A CMOS instrumentation amplifier with 90-dB CMRR at 2-MHz using capacitive neutralization: Analysis, design considerations, and implementation," vol. 58, no. 4, pp. 699–710, 2011.

[2] S. Hong, K. Lee, U. Ha, H. Kim, Y. Lee, Y. Kim, and H.-J. Yoo, "A 4.9 mΩ-sensitivity mobile electrical impedance tomography IC for early breast-cancer detection system," vol. 50, no. 1, pp. 245–257, 2015.

[3] R. J. Halter, A. Hartov, and K. D. Paulsen, "A broadband high-frequency electrical impedance tomography system for breast imaging," *Biomedical Engineering, IEEE Transactions on*, vol. 55, no. 2, pp. 650–659, 2008.

[4] N. Van Helleputte, S. Kim, H. Kim, J. P. Kim, C. Van Hoof, and R. Yazicioglu, "A 160 μA biopotential acquisition IC with fully integrated ia and motion artifact suppression," vol. 6, no. 6, pp. 552–561, 2012.

[5] Y.-C. Teng and K. Odame, "A 10 MHz 85 dB dynamic range instrumentation amplifier for electrical impedance tomography," in *Biomedical Circuits and Systems Conference (BioCAS), 2014 IEEE*, 2014, pp. 632–635.

[6] B. Wilson, "Universal conveyor instrumentation amplifier," *Electronics Letters*, vol. 25, no. 7, pp. 470–471, 1989.

[7] R. Yazicioglu, P. Merken, R. Puers, and C. Van Hoof, "A 200μW eight-channel acquisition ASIC for ambulatory EEG systems," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, 2008, pp. 164–603.

[8] N. Klemmer, "Low power class ab unity gain buffer circuit," US Patent 6,124,740, Sep. 26, 2000.