A High Frequency, High Frame Rate Front End for Electrical Impedance Tomography

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***Abstract*—Electrical impedance tomography (EIT) is an imaging modality that takes spectral images of the tissue under study. The EIT imaging approach, compared to the other imaging techniques such as X-ray, offers an affordable, non-ionizing portable device for home health monitoring. A front-end with high frame rate that covers a wide range of frequencies is essential for such applications. This paper presents the circuit design and implementation of a high frequency, high frame rate front-end for electrical impedance tomography system. The proposed front-end comprises a wide bandwidth programmable gain instrumentation amplifier, a mega-sample per second analog-to-digital converter (ADC), and an ADC driver. The read-out channel is designed and fabricated in a 0.18 μm CMOS technology. The measurement results show that the proposed front-end covers the wide frequency range of 100 Hz to 10 MHz, with a frame rate of 30 frames per second for a 16-electrode system, with an average signal-to-noise ratio of more than 60 dB. The entire read-out channel consumes between 6.9 mW and 21.8 mW based on its operation frequency.**

I. INTRODUCTION

Early stage detection and treatment of chronic diseases can help the health care professionals to react in a proactive, rather than reactive manner. Introducing mobile health (m-health) and telemonitoring devices, not only helps early stage diagnosis, it also helps health care professionals to follow up on patients' post operative status. The electrical impedance tomography (EIT) compared to the traditional imaging modalities, such as X-ray and MRI, has several advantages including: its radiation-free nature, its affordability, and its potential to be miniaturizable [1], [2]. These features make the EIT approach a viable option for use in telemonitoring devices [3], [4].

For a wearable EIT system, there are various design requirements that the read-out circuit (which is used to read and digitize the boundary voltages) must meet. The frame rate, which is the speed at which successive images can be taken, must be maximized to reduce the effects of patients' movement and electrode displacement [5]. To increase contrast and sensitivity in applications like breast cancer detection [6] and acute stroke imaging [7], interrogation frequencies of higher than 1 MHz are needed. Finally, to enable battery operation and portability, low power and small form factor are also necessary.

Several EIT solutions have been introduced to date [3], [4], [8], [9], but none of them meets our specifications of 10 MHz bandwidth, 30 frames per second (fps) and small form factor.

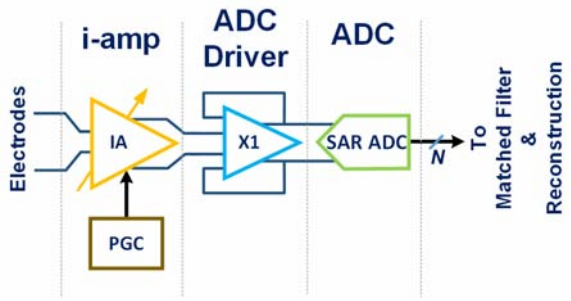

Fig. 1. Block diagram of the proposed read-out channel, including a wide bandwidth IA, a programmable gain control (PGC) unit, an ADC driver buffering the IA output, and a SAR ADC. The digital output of the ADC is fed to a digital matched filter to extract the amplitude and phase of the signal, which can later be processed by the reconstruction algorithm.

In this work, we present an application specific integrated circuit (ASIC) read-out channel that is suitable for small form factor EIT. We use a wide-band instrumentation amplifier (IA) to achieve high frequency operation, and we use a mega-sample rate analog-to-digital converter (ADC) to achieve high frame rate. The proposed read-out chain operates over the frequency range of 100 Hz to 10 MHz, with a frame rate of 30 fps for a 16-electrode system, with an average signal-to-noise ratio (SNR) of more than 60 dB.

II. SYSTEM DESIGN

In this section, circuit implementation of the main building blocks of the read-out channel are presented. Fig. 1 shows the block diagram of the proposed read-out channel, including an IA, a programmable gain control (PGC) unit, an ADC driver, and a SAR ADC. We implemented each of these components to meet our target design goals of high frame rate, high signal-to-noise ratio, and wide interrogation frequency range, with low power consumption.

A. Hybrid R-C Successive-approximation-register ADC

To achieve the high frame rate for the EIT system, the ADC requires a sample rate in the mega-sample per second (MSPS) range. The presence of the matched filter at the back-end of the read-out channel (Fig. 1) gives us different sets of choices for the speed and resolution of the ADC, all meeting the required SNR, and frame rate of the EIT system [10]. Among this set of choices, 12-bit, 6.25 MSPS SAR ADC was

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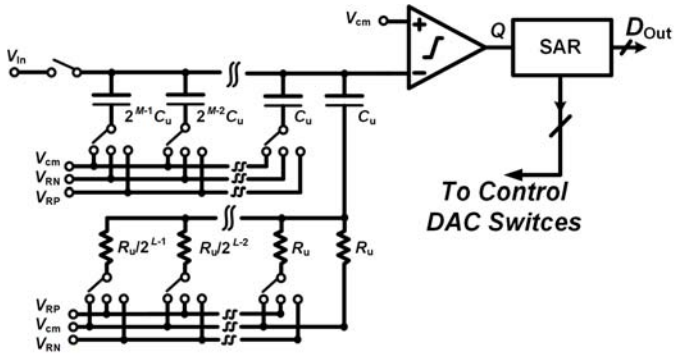


Fig. 2. Simplified single-ended circuit schematic of the hybrid R-C SAR ADC, comprising an M-bit charge redistribution capacitive DAC for the most significant bits (MSBs), and L-bit voltage scaling resistive DAC for the least significant bits (LSBs), resulting in an N-bit $(M + L)$ ADC [11].

chosen to be implemented based on the available technology and considering the power dissipation of the ADC.

We achieve a MSPS sampling rate with a hybrid resistive-capacitive (R-C) SAR ADC. This structure reduces the size of the capacitive DAC [11], [12], and hence the required time for charging and discharging the capacitors. This enables us to achieve the mega samples-per-second rate.

The SAR ADC is implemented differentially and its simplified single-ended circuit schematic is shown in Fig. 2.

For the chain to process a 10 MHz signal, one option is to have an ADC with a sampling frequency of at least 20 MHz (according to the Nyquist theorem). However, this comes at the price of high power consumption. Instead, we implemented the ADC with a lower sampling frequency, and employed an under-sampling technique to avoid excessive power consumption. The ADC samples the input signal in two regions: up to the Nyquist rate of the ADC, 3.125 MHz, the input signal is sampled in a normal fashion, and above 3.125 MHz the under-sampling technique was used to process the high frequency signals. In the under-sampling approach [13], the input signal is aliased back to a frequency equal to $\mid f_{\text{in}} - nF_{\text{s}} \mid$, where n is an integer number, and f_{in} and F_{s} are respectively input and sampling frequencies. Fig. 3 illustrates

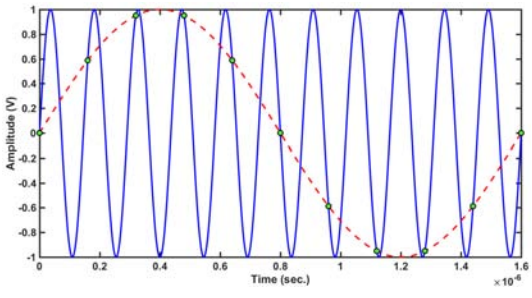


Fig. 3. Illustration of the under-sampling technique in time domain. The solid blue line shows the input signal at 6.875 MHz. The input signal is sampled at 6.25 MHz and the dashed red line represents the result. The sampled signal appears at a much lower frequency of 625 kHz, which lies in the fist Nyquist zone of the ADC.

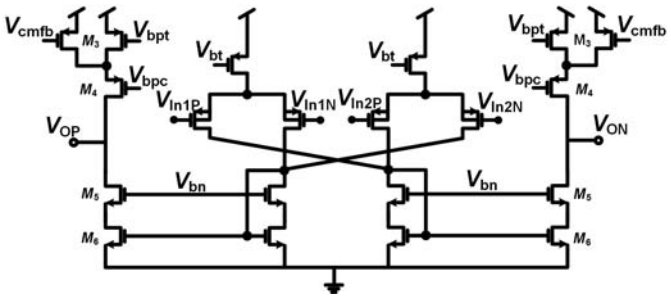


Fig. 4. ADC driver implemented as a fully differential difference amplifier.

the under-sampling approach, where a 6.875 MHz signal (solid line) is sampled at 6.25 MHz. The sampled signal (dashed line) appears as a low frequency signal at 625 kHz (=6.875 MHz - 1×6.25 MHz). Therefore, by employing the under-sampling technique for a high frequency signal, one can process a much lower frequency signal that aliases back to the first Nyquist zone of the ADC.

The sampling frequency of the ADC is adaptive and varies based on the frequency of the input signal. Therefore, the power consumption of the ADC ranges from 2.19 mW at 6.25 MSPS to 0.81 mW at 160 kSPS. By reducing the sampling rate of the ADC, the speed and bandwidth requirements of the ADC driver can be relaxed for low frequency input signals.

B. ADC Driver

Due to the limited current driving capability of the IA block, an ADC driver is placed between the IA and the ADC. Fig. 4 shows the core of the ADC driver, which comprises a fully differential difference amplifier (FDDA) and a common mode feedback (CMFB) block (not shown in the figure).

Measurement results show that the ADC driver consumes 1.64 mW and 15.1 mW, respectively, when the sampling frequency of the ADC is set to 160 kHz and 6.25 MHz, and linearly increases for the frequencies in between. The issue of power optimization of the ADC driver will be addressed in subsequent design iterations.

C. Instrumentation Amplifier

Among different structures available for the instrumentation amplifier block, the current conveyor based, open-loop IA was chosen, which is most suitable for wide bandwidth applications [14], [15]. In order to relax the resolution requirement of the ADC, and therefore reduce the ADC's power consumption, the IA block has different gain settings for different input levels. The implemented current conveyor based IA is amenable to programmable gain settings.

The schematic of the implemented IA core is shown in Fig. 5, which comprises a transconductance stage at the input stage, and a transimpedance stage at the output stage. In the transconductance stage, the input voltage is buffered with two source follower transistors, $M_{1\text{L}}$ and $M_{1\text{R}}$. The buffered voltage is then converted into current through the R_1 resistor. Two current sources at the bottom, $M_{4\text{L,R}}$, supply a fixed current for the input transistors. Therefore, any current that flows

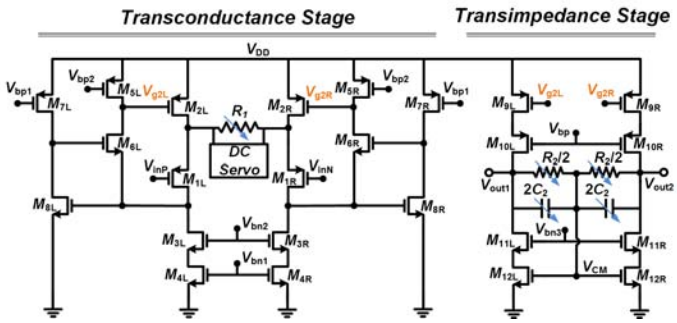


Fig. 5. Circuit schematic of the instrumentation amplifier core, which is implemented fully differentially and comprises two stages. The first stage is the transconductance stage, converting the input signal into current and mirroring it to the next stage. The second stage performs as a transimpedance stage, converting the mirrored current back into voltage.

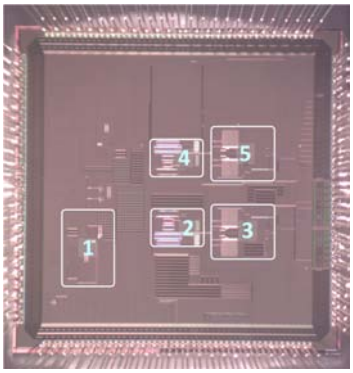


Fig. 6. Die photograph of the read-out chain showing the labeled blocks as follows: (1) instrumentation amplifier with the programmable gain control unit and the anti-aliasing filter, (2) main ADC driver, (3) main hybrid R-C SAR ADC, (4) testing ADC driver, and (5) testing SAR ADC blocks.

through R_1 should be supplied by the top transistors, $M_{2\text{L,R}}$. The current passed through $M_{2\text{L,R}}$ is then mirrored to the transimpedance stage through $M_{9\text{L,R}}$. In the transimpedance stage, the current is again converted back to voltage through the R_2 resistor.

The gain of the IA is approximately R_2/R_1, which in this design is programmable to three different settings, based on the amplitude of the input signal. The R_2 resistor also acts as a resistive feedback to stabilize the DC voltage of the output nodes by properly biasing the $M_{12\text{L,R}}$ NMOS transistors. A bank of capacitors (C_2) is placed in parallel with the resistor R_2 in the transimpedance stage, which together act as a low pass/anti-aliasing filter with the cut-off frequency of $(1/R_2C_2)$. The low pass filter has programmable cut-off frequencies, which can be selected based on the frequency of the input signal.

The instrumentation amplifier consumes 4.51 mW power from 3.3 V power supply, and covers the frequency range of 100 Hz to 10 MHz.

III. MEASUREMENT RESULTS

The proposed read-out channel was fabricated in 0.18 μm CMOS technology. A die photograph of the fabricated chip is shown in Fig. 6.

The signal-to-noise ratio (SNR) of an EIT system shows the noise content of the measurements, and is a metric of how precise and replicable the measurements are. The SNR of an EIT system is evaluated by performing repeated measurements of an applied signal to the chain while the measurement conditions are kept unchanged [8]. The extracted amplitude of the matched filter at the back-end of the read-out channel is recorded, and the SNR can be calculated as the ratio of the mean squared over the variance of the repeated measurements:

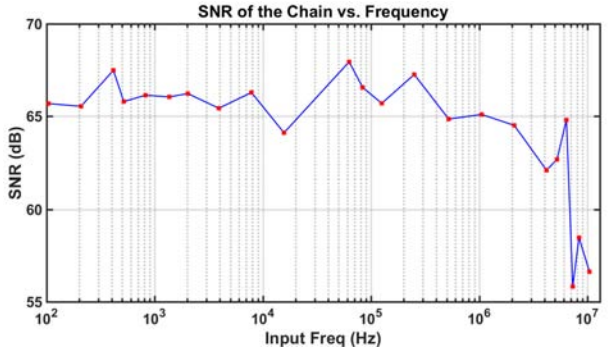
$$\begin{aligned}\text{SNR} &= 10\log_{10}\left(\frac{\overline{V}^2}{\text{var}(V)}\right)\\ &= 10\log_{10}\left(\frac{1}{N}\frac{\left(\sum_{n=1}^{N}V_n\right)^2}{\sum_{n=1}^{N}\left(V_n-\overline{V}\right)^2}\right)\end{aligned} \quad (1)$$

where N is the number of repeated measurements, $\overline{V}$ represents the mean of all measurements, and V_n is the value of the n-th measurement.

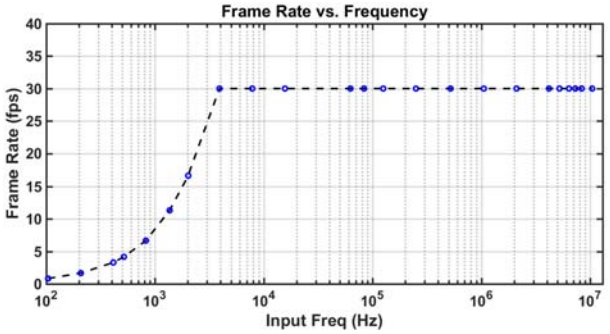
The SNR measurements were performed for 23 different frequencies ranging from 100 Hz to 10 MHz with 60 repeated measurements for each frequency ($N = 60$). The SNR was then calculated for each frequency using (1). The measured SNR versus frequency is plotted in Fig. 7 (a). Fig. 7 (b) shows the frame rate of the front-end versus frequency. We designed the front-end for use in a 16-electrode system. With 16 electrodes and a tetrapolar current injection pattern, $16\,(16-1)\,/2 = 120$ independent measurements are required to have one frame [2]. Having a target of maximum 30 frames per second mandates that each measurement needs to take no longer than 278 μs $(= 1/\,(120 \times 30))$. Fig. 7 (b) shows that for the input frequency signals between 3.6 kHz and 10 MHz, the frame rate is constant and equal to 30 fps. For frequencies lower than 3.6 kHz, the frame rate drops. This is because the matched filter requires a whole number of periods to extract the amplitude/phase [16], and for such low frequency signals one period of the input signal is longer than 278 μs. The lower the input frequency, the longer the period of the signal, which demonstrates why the frame rate drops for input frequencies lower than 3.6 kHz.

The performance comparison of the proposed ASIC with previous, state-of-the-art works is presented in Table I.

The power dissipation in Table I shows the approximate power consumption of front-end per channel for each system. In our design, we employed the current conveyor based IA, which is well suited for high speed, low power, wide



(a)



(b)

Fig. 7. (a) SNR of the read-out chain versus frequency, measured by performing repeated measurements using (1) with the frequency range of 100 Hz to 10 MHz, and (b) frame rate of the read-out chain versus frequency considering a system employing 16 electrodes with tetrapolar injection current pattern.

bandwidth applications. We also employed mega-sample rate ADC in our proposed chain to achieve rapid data acquisition.

IV. CONCLUSION

The design and implementation of a high frequency, high frame-rate front-end was presented for use in electrical impedance tomography imaging system. The read-out chain is composed of a wide bandwidth programmable gain instrumentation amplifier, an ADC driver, and a mega-sample per second hybrid R-C SAR ADC. The proposed front-end was designed and fabricated in a 0.18 μm CMOS technology. The measurement results of the read-out channel show an average SNR of more than 60 dB with a maximum frame rate of 30 fps, while covering a wide frequency range of 100 Hz to 10 MHz. The entire read-out channel, consumes between 6.9 mW and 21.8 mW, depending on its frequency of operation.

TABLE I
COMPARISON TABLE FOR EIT CUSTOM IC ANALOG FRONT-ENDS

	ESSCIRC'11 [9]	*JSSC'15 [3]*	*This Work*
Process	0.6 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Frequency	10 kHz $\sim$ 1 MHz	10 $\sim$ 200 kHz	100 Hz - 10 MHz
Extracted Data	Amplitude & Phase	Amplitude & Phase	Amplitude & Phase
Demodulation Type	Analog	Analog	Digital
SNR (Average)	N/A	56.3 dB	64.4 dB
Power	5 mW †	1.73 mW †	6.9 mW$\leq$P$\leq$21.8 mW

† Includes current injection block.

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