

# A 10 MHz 85 dB Dynamic Range Instrumentation Amplifier for Electrical Impedance Tomography

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**Abstract**—In this paper, we present an instrumentation amplifier for high speed electrical impedance tomography. The instrumentation amplifier includes a fast acting automatic gain control, which allows it to process a wide dynamic range of input signals with low power consumption and without sacrificing the frame rate of the tomography system. The instrumentation amplifier was designed in a 3.3 V, 180 nm CMOS process. Simulation results show that it has a dynamic range of 85 dB over a 10 MHz bandwidth, with a total power consumption of 3.1 mW.

## I. INTRODUCTION

Patients with chronic heart disease are at risk of suffering an episode of acute decompensated heart failure [1]. If the patient’s cardiac hemodynamic status could be remotely monitored, then this would permit early intervention, potentially avoiding hospitalization and other adverse outcomes [2]. One promising technology for enabling such cardiac monitoring at home is electrical impedance tomography (EIT) [3], [4].

EIT is attractive because it is low cost, non-ionizing and amenable to miniaturization [5], [6]. The challenge, however, is that high quality EIT imaging requires an analog front end that operates from 100 Hz to 10 MHz, has a dynamic range of over 80 dB and provides the maximum possible frame rate for any given interrogation frequency [7]. Power consumption is an additional concern; for a wearable, 128 electrode EIT system, each channel of the analog front end should consume on the order of 1 mW of power.

In this paper, we present an instrumentation amplifier that is part of an EIT system-on-chip that we are developing for a remote cardiac monitoring application. Our instrumentation amplifier (i-amp) uses a fast acting automatic gain control (AGC) loop to achieve high dynamic range with low power consumption, while providing close to the maximum theoretical frame rate at any interrogation frequency from 100 Hz to 10 MHz.

## II. SYSTEM OVERVIEW

Figure 1 shows a simplified block diagram of one channel of the analog front end of our EIT system. The current source injects approximately one period of a sinusoidal signal into the tissue, via a pair of electrodes and DC blocking capacitors (for patient safety). The resulting boundary voltages are measured via another set of electrodes and capacitors and amplified by an i-amp. The gain of the i-amp is variable and is controlled by an AGC unit. Since each voltage reading lasts for about

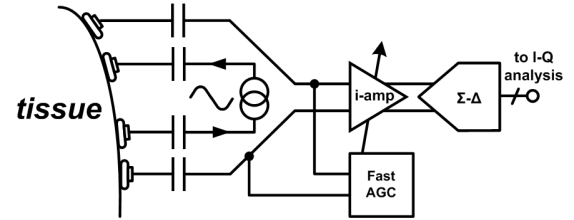


Fig. 1: Simplified analog front end signal chain for electrical impedance tomography.

one period, the AGC unit must output a valid control signal within a fraction of this time, or else the system’s frame rate will fall. The output of the i-amp is fed to a  $\Sigma$ - $\Delta$  ADC, and the digitized signal undergoes an I/Q analysis, from which are extracted its amplitude and phase. The amplitude and phase readings from different current injection patterns are used to reconstruct a tomography-like impedance map of the tissue under test.

## III. INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is based on the universal current conveyor instrumentation amplifier, which provides a high common mode rejection ratio and is also amenable to programmable gain [8]. As shown in Fig. 2a, it consists of a transconductance stage and a transimpedance stage of variable gain.

The transconductance stage is a pair of flipped voltage followers with voltage gain boosting [9] and a variable resistor,  $R_1$ . Input transistors  $M_1$  and  $M_9$  serve as source voltage followers, with their drain voltages held fixed by the gain boosting stages (see Fig. 2b). Holding the drain voltages of transistors  $M_1$  and  $M_9$  fixed minimizes the effect of channel length modulation, and also keeps the transistors in saturation even during large input swings. The input AC signal is buffered from the gates of  $M_1$  and  $M_9$  to their sources, causing a voltage drop to appear across resistor  $R_1$ . The resulting input-dependent current through  $R_1$  is sourced/sunk by transistors  $M_2$  and  $M_{10}$ , and is thus mirrored to transistors  $M_8$  and  $M_{16}$  in the transimpedance stage. Transistors  $M_8$  and  $M_{16}$  force the mirrored current to flow through  $R_2$ , and the voltage across  $R_2$  is the i-amp output. Assuming 1:1 current mirroring, the differential voltage gain of the i-amp is given as  $R_2/R_1$ . Different gain settings can be programmed by switching in

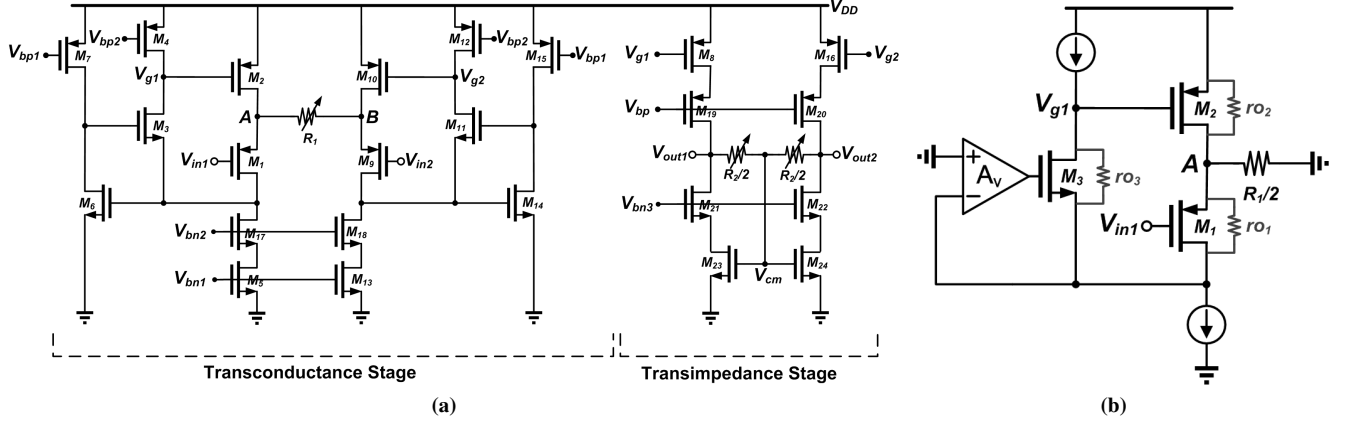


Fig. 2: (a) Circuit diagram of the instrumentation amplifier core. The resistance values of  $R_1$  and  $R_2$  depend on the output code of the amplitude detector. (b) Simplified small-signal half circuit of i-amp transconductance stage.  $A_v$  represents the common source amplifier formed by transistors  $M_6$  and  $M_7$ ; along with the  $M_3$  common source amplifier,  $A_v$  pins the drain of  $M_1$  to ac ground.

different ratios of  $R_1$  and  $R_2$ . The speed, power consumption and noise of the i-amp depend on the absolute values of  $R_1$  and  $R_2$ .

The speed of the i-amp is determined by the dominant pole that is due to the output node. The resistance at this node is approximately  $R_2/2$ , which can be expected to have a much smaller value than that of the output cascode transistors. The dominant pole is therefore approximately equal to  $2/(R_2 C_L)$ , where  $C_L$  is the output load capacitance. In our system, the load capacitance will be dominated by the input of an ADC driver, and is on the order of 125 fF.

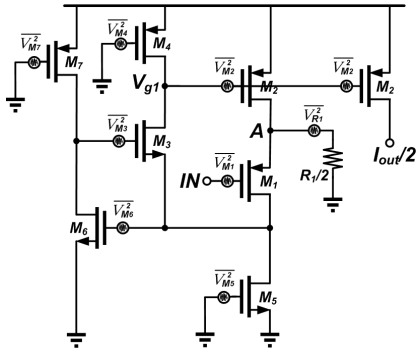


Fig. 3: Half circuit of the i-amp transconductance stage used for noise analysis.

The input stage of the i-amp produces the majority of the circuit noise. Similar to the approach described in [10], the schematic of Fig. 3 is the equivalent half circuit of the i-amp's input stage that we used for calculating the input referred voltage noise power spectral density (PSD). It is given as

$$\begin{aligned} \overline{V}_{IN}^2 &= 2\overline{V}_{M_1}^2 + \overline{V}_{R_1}^2 + \overline{V}_{M_5}^2 \frac{g_{m_5}^2}{4g_{m_1}^2} (g_{m_1} R_1 + 2)^2 \\ &+ \left( \overline{V}_{M_3}^2 g_{m_3}^2 + \overline{V}_{M_4}^2 g_{m_4}^2 \right) g_{m_2}^2 (r_{o_3} \parallel r_{o_4})^2 \frac{R_1^2}{2} \end{aligned}$$

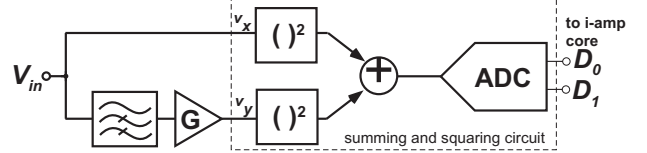


Fig. 4: Block diagram of fast automatic gain control unit.

$$\begin{aligned} &+ \overline{V}_{M_6}^2 g_{m_6}^2 g_{m_3}^2 (r_{o_6} \parallel r_{o_7})^2 g_{m_2}^2 (r_{o_3} \parallel r_{o_4})^2 \frac{R_1^2}{2} \\ &+ \overline{V}_{M_7}^2 g_{m_7}^2 g_{m_3}^2 (r_{o_6} \parallel r_{o_7})^2 g_{m_2}^2 (r_{o_3} \parallel r_{o_4})^2 \frac{R_1^2}{2} \\ &+ \overline{V}_{M_2}^2 g_{m_2}^2 R_1^2, \end{aligned} \quad (1)$$

where  $\overline{V}_{M_x}^2$  and  $g_{m_x}$  are the voltage noise PSD and small signal transconductance of transistor  $M_x$ , respectively. Also,  $\overline{V}_{R_1}^2$  is the voltage noise PSD of resistor  $R_1$ . The noise is minimized by ensuring that the input transistors have large transconductances relative to the current source transistors, and that the value of  $R_1$  is as low as possible. However, for a given input amplitude, smaller values of  $R_1$  generate larger currents through it, which must be supported by  $M_2$  and  $M_{10}$  having larger quiescent currents. We have found that a choice of  $10 \text{ k}\Omega \geq R_1 \geq V_{inpp}/(200 \mu\text{A})$ , where  $V_{inpp}$  is the peak-to-peak input signal amplitude, produces a good balance between noise performance and current consumption.

#### IV. FAST AUTOMATIC GAIN CONTROL

To maintain the frame-rate of the system, the correct gain setting must be determined within a fraction of a period of the input signal. Envelope detection is not a suitable solution, because it relies on a low pass filter with a slow transient response. Directly comparing the level of the signal to a set threshold is also unsuitable, because there is no a priori knowledge about the signal's phase. The approach we take

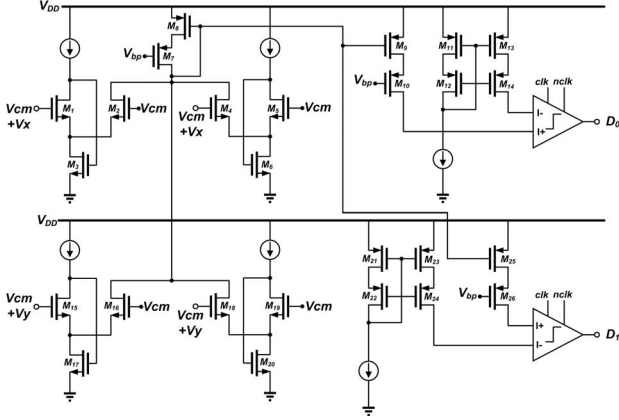


Fig. 5: Squaring and summing circuit. The input signals  $v_x$  and  $v_y$  are converted to a current via a square law and summed via KCL on the drain of  $M_7$ . The current-mode comparators are used to generate a two bit output code.

is to perform a fast amplitude detection [11], which can be calculated via the expression

$$A^2 = x^2 + \dot{x}^2/\omega^2, \quad (2)$$

where  $x = A \sin(\omega t)$  is the input signal.

Figure 4 shows a block level implementation of Eqn. (2). The high pass filter, implemented as a first order OTA-C filter, produces the derivative term,  $\dot{x}$ . Changing the bias current of the OTA programs the break frequency of the high pass. The break frequency is programmed to be 100 times the frequency of the input signal; a lower break frequency would degrade the differentiating operation of the filter, while a higher break frequency would excessively amplify high frequency noise relative to the input signal. With the chosen break frequency, the high pass filter attenuates the signal by approximately 100. We restore the amplitude of the high-passed signal with the gain block,  $G$ , which is implemented as an OTA-resistive load amplifier [12].

The squaring and summing operation in Eqn. (2) is implemented using two pairs of flipped source followers, as shown in Fig. 5. Given the low accuracy required of the amplitude detector, the squaring circuit can be operated either in above- or subthreshold saturation. However, if we assume an above threshold, square law characteristic, then, ignoring the body effect, the drain currents of transistors  $M_{2,4,16,18}$  in Fig. 5 are

$$\begin{aligned} I_{2,4} &= K(V_{cm} \mp v_x + V_s - V_T)^2 \\ I_{16,18} &= K(V_{cm} \mp v_y + V_s - V_T)^2, \end{aligned} \quad (3)$$

where  $V_{cm}$  and  $V_s$  are the transistor gate and source DC voltages, respectively, while  $v_x$  and  $v_y$  represent the  $x$  and  $\dot{x}/\omega$  signals, respectively, from Eqn. (2). Also,  $V_T$  is the threshold voltage. The currents of Eqn. (3) are summed onto the drain of transistor  $M_7$  in Fig. 5; the resulting drain current is a sum of the  $v_x^2$  and  $v_y^2$  terms as desired, plus a constant offset. This current is input to two current-mode comparators, which are based on the track and hold latch described in [13]. The 2

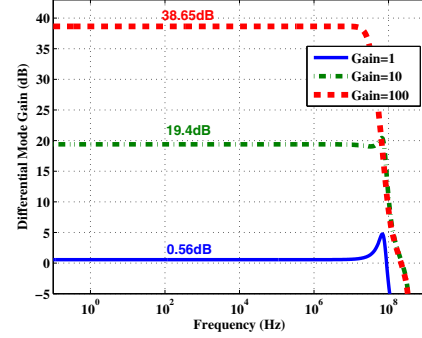


Fig. 6: Magnitude frequency response of the i-amp for different gain settings. The nominal gain settings, determined by the  $R_2/R_1$  ratio, differ slightly from the actual observed gains.

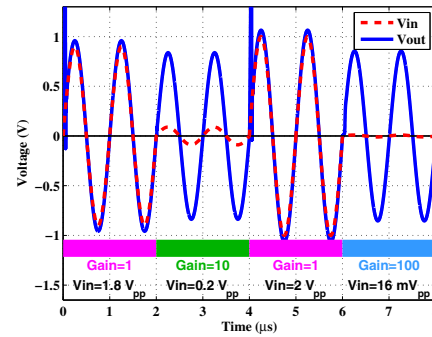


Fig. 7: Operation of the fast AGC for a 1 MHz input signal. The glitches at the beginning of the input amplitude transitions are due to invalid AGC outputs, but they last for only 30 ns, which is 3% of the length of the period.

bit output of the comparator pair is used to control the gain setting of the instrumentation amplifier.

## V. RESULTS

We designed the adaptive gain instrumentation amplifier in a 3.3 V, 180 nm CMOS process. We used foundry-provided test data and models in simulations, to verify that the circuit would work as desired when fabricated.

The magnitude frequency response plots in Fig. 6 show that the gain of the instrumentation amplifier is selectable at 0.5, 19 and 38 dB. For each of these settings, the amplifier maintains its gain over a bandwidth of 30 MHz or more. The current consumption of the i-amp core is 945  $\mu$ A, while the current consumption of the fast AGC is 25  $\mu$ A. With a 3.3 V power supply, this gives a total power consumption of 3.1 mW.

Figure 7 shows the fast AGC in operation. It has an attack time that is 3% of the 1 MHz period. The attack time takes a similar fraction of the period for lower frequency inputs, but it rises to 30% of the period for a 10 MHz signal. In addition to the fast attack time, the AGC is insensitive to the phase of the input signal, as confirmed by the results shown in Fig. 8.

The i-amp exhibits input offset due to threshold voltage

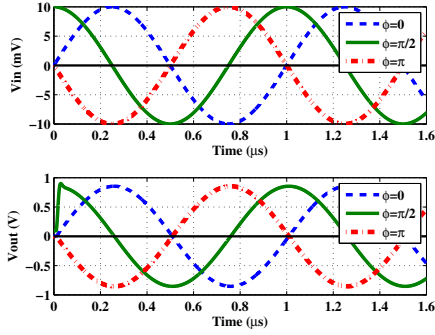


Fig. 8: I-amp response to 10 mV, 1 MHz signals. The AGC converges within 30 ns, regardless of the input signal’s phase.

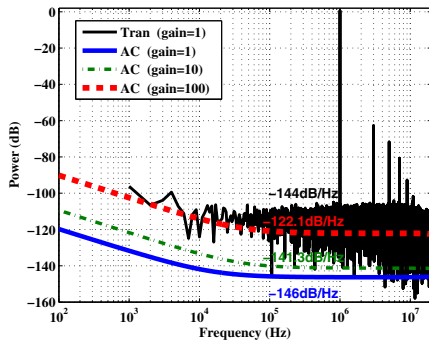


Fig. 9: FFT of the i-amp output when processing a  $2 V_{pp}$ , 1 MHz input (black curve). Lines labelled ‘AC’ are the results of ac noise analyses (output-referred) for different gain settings.

mismatch between its input transistors ( $M_1$  and  $M_9$  of Fig. 2a), which results in harmonic distortion, as shown in Fig. 9. The total harmonic distortion of the i-amp is between 0.66% and 1.7%, depending on the input signal’s amplitude and frequency. Another implication of input offset is a non-zero common mode gain; with careful layout, we can achieve a common mode rejection ratio (CMRR) of over 120 dB. In the extremely unlikely scenario that the input offset equals 3 times the standard deviation in threshold voltage mismatch, Fig. 10 shows that the CMRR ranges from 63 to 75 dB.

Figure 9 also shows the i-amp’s output referred noise power spectral density (PSD) for different gain settings. Integrating the PSD from 100 Hz to 20 MHz, the maximum achievable SNR is 71 dB, for an input amplitude of  $2 V_{pp}$ . Due to the AGC, the dynamic range is extended to 85 dB.

## VI. CONCLUSION

We have presented an instrumentation amplifier for the voltage readout of an EIT system that can process inputs up to an amplitude of  $2 V_{pp}$ , and over a frequency range of 100 Hz to 10 MHz. The instrumentation amplifier uses a fast AGC scheme to achieve a maximum SNR of 71 dB and a dynamic range of 85 dB while consuming 3.1 mW of power.

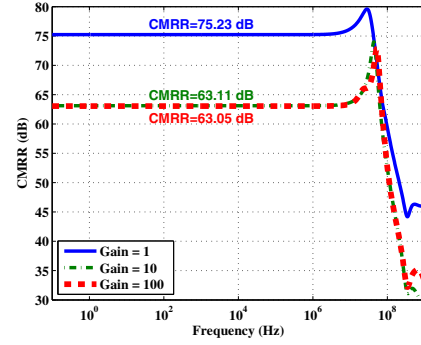


Fig. 10: Effect of extreme input offset voltage (i.e.  $3\sigma(\Delta V_T)$ ) on common mode rejection ratio.

## ACKNOWLEDGMENT

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## REFERENCES

- [1] Javed Butler, Diana Chirovsky, Hemant Phatak, Anne McNeill, and Robert Cody, “Renal function, health outcomes, and resource utilization in acute heart failure a systematic review,” *Circulation: Heart Failure*, vol. 3, no. 6, pp. 726–745, 2010.
- [2] Ayesha Hasan and Vince Paul, “Telemonitoring in chronic heart failure,” *European heart journal*, vol. 32, no. 12, pp. 1457–1464, 2011.
- [3] Anton Vonk-Noordegraaf, André Janse, Johan T Marcus, Jean GF Bronzwaer, Pieter E Postmus, Theo JC Faes, and Peter MJM de Vries, “Determination of stroke volume by means of electrical impedance tomography,” *Physiological measurement*, vol. 21, no. 2, pp. 285, 2000.
- [4] Robert Gail Billings, Justin S Clark, Allan L Kaminsky, Jon Neese, and Ke-shiang Yang, “System and method for in-vivo hematocrit measurement using impedance and pressure plethysmography,” Oct. 3 2000, US Patent 6,128,518.
- [5] Iasonas F Triantis, Andreas Demosthenous, Mohamad Rahal, Hongwei Hong, and Richard Bayford, “A multi-frequency bioimpedance measurement ASIC for electrical impedance tomography,” in *ESSCIRC (ESSCIRC), 2011 Proceedings of the. IEEE*, 2011, pp. 331–334.
- [6] Sunjoo Hong, Kwonjoon Lee, Unsoo Ha, Hyunki Kim, Yongsu Lee, Youchang Kim, and Hoi-Jun Yoo, “A 4.9 mΩ-sensitivity mobile electrical impedance tomography ic for early breast-cancer detection system,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International. IEEE*, 2014, pp. 316–317.
- [7] Ryan J Halter, Alex Hartov, and Keith D Paulsen, “A broadband high-frequency electrical impedance tomography system for breast imaging,” *Biomedical Engineering, IEEE Transactions on*, vol. 55, no. 2, pp. 650–659, 2008.
- [8] B Wilson, “Universal conveyor instrumentation amplifier,” *Electronics letters*, vol. 25, no. 7, pp. 470–471, 1989.
- [9] Vadim V Ivanov and Igor M Filanovsky, *Operational Amplifier Speed and Accuracy Improvement: Analog Circuit Design with Structural Methodology*, Boston, MA: Springer US, 2004.
- [10] Refet Firat Yazicioglu, Sunyoung Kim, Tom Torfs, Patrick Merken, and Chris Van Hoof, “A 30μw analog signal processor ASIC for biomedical signal monitoring,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International. IEEE*, 2010, pp. 124–125.
- [11] Alexander M Zayezdny, Yehoshua Adler, and Ilan Druckmann, “Short time measurement of frequency and amplitude in the presence of noise,” *Instrumentation and Measurement, IEEE Transactions on*, vol. 41, no. 3, pp. 397–402, 1992.
- [12] Jianhong Xiao, Iuri Mehr, and Jose Silva-Martinez, “A high dynamic range CMOS variable gain amplifier for mobile DTV tuner,” *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 2, pp. 292–301, 2007.
- [13] Akira Yukawa, “A CMOS 8-bit high-speed A/D converter IC,” *Solid-State Circuits, IEEE Journal of*, vol. 20, no. 3, pp. 775–779, 1985.