January 2013

Joseph R. Cavallaro

Professor
Rice University, MS 380
Dept. of Electrical & Computer Engineering
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Education

Cornell University, Ph.D. in Electrical Engineering, August 1988.
Thesis Title: VLSI CORDIC Processor Architectures for the Singular Value Decomposition.
Thesis Advisor: Franklin T. Luk.

Princeton University, M.S. in Electrical Engineering, June 1982.

University of Pennsylvania, B.S. in Electrical Engineering, *(magna cum laude)*, May 1981.

Positions

- 2002-Present Rice University, Professor, Electrical & Computer Engineering
- 2000-Present Rice University, Courtesy appointment in Computer Science Dept.
- 2007-Present University of Oulu, Finland, Docent, (Adjunct Professor)
- 2004-2005 University of Oulu, Finland, Visiting Professor, Spring 2005
- 1994-2002 Rice University, Associate Professor (Tenured), Electrical & Computer Engineering
- 1996-1997 National Science Foundation, Program Director, Systems Prototyping and Fabrication Program, MIPS Division, CISE Directorate
- 1988-1994 Rice University, Assistant Professor, Electrical & Computer Engineering
- 1987-1988 Cornell University, IBM Graduate Fellow
- 1986-1987 Cornell University, Research Assistant
- 1983-1986 Cornell University, Teaching Assistant
- 1981-1983 AT&T Bell Laboratories, MTS, Special Business Services Lab.

Honors and Awards

- IEEE Circuits and Systems Society Distinguished Lecturer, 2012-2013
- SDR Forum Outstanding Paper Award, (with K. Amiri, C. Dick, R. Rao), 2010.
- IEEE Great Lakes Symposium on VLSI Best Paper Award, (with Y. Sun), 2009.
- IEEE International SoC Conference, Best Paper Award, (with Y. Sun), 2008.

- IEEE Workshop on Signal Processing Systems, (SiPS), Bob Owens Memorial Paper Award, (with Y. Sun), 2008.
- Fulbright Senior Specialists Program Roster, 2004-2008
- Nokia Foundation, Visiting Professor Fellowship, 2004-2005
- IEEE Computer Society Distinguished Lecturer, 2004-2006
- IEEE Application-Specific Systems, Architectures and Processors Conference, Best Paper Award, (with B. Haller and J. Götze), 1997.
- IEEE Circuits and Systems Society Chapter of the Year Award, (accepted as Chair of the Houston Chapter), 1996
- Hershel M. Rich Invention Award, Rice Engineering Alumni, 1994
- IEEE Region 5 Award for service as Student Branch Counselor, 1992
- NSF Research Initiation Award, 1989-1992
- IBM Graduate Fellowship, 1987-1988
- AT&T Graduate Study Program, 1981-1982
- Member of Tau Beta Pi and Eta Kappa Nu
- National Merit Scholarship, 1977-1978

Research Interests

- VLSI DSP architectures and parallel algorithms for wireless communications and robotics
- VLSI systems design and microlithography
- Fault-Tolerant robotic and computer systems
- High-speed computer arithmetic

Recent Research Grants

1. "US-Ireland Partnership: WiPhyLoc8: Dynamic WiFi Positioning using Physical Layer Parameters for Location-based Services and Security," NSF ENG ECCS (PI), (with R. Woods, Queen's University Belfast, C. Bleakley, University College Dublin).
2. "A Comprehensive Study of Wireless Network Systems: Algorithms, Architectures, and Analog Devices for Full-duplex Systems and Coding for Networks," Renesas Mobile Europe Inc., (Co-PI), 230,000 Euro, 2012, (with B. Aazhang (PI), A. Babakhani).
3. "System Power Optimization of Mobile Systems," Samsung Telecommunications, Inc., $75,000, 2011, (with L. Zhong).
4. "Context Aware Wireless Networks: Algorithms, Architectures, and Applications," Renesas Mobile Europe Inc., (Co-PI), 170,000 Euro, 2011, (with B. Aazhang (PI)).
5. "Multi-mode Receiver and Decoder Architectures for UMTS/LTE Systems," Huawei Inc. (PI), $160,000, 2010-2011.
6. "Leadership University Program: New Applications for DSPs in Mobile Health and Neuroengineering" Texas Instruments, Inc., (Co-PI), $1,000,000, 2011-2013, (C. S. Burrus, B. Aazhang, J. R. Cavallaro, E. W. Knightly, R. G. Baraniuk, M. Orchard).
7. "Collaborative Research: MRI: Development of mobileWARP - A Platform for Next-Generation Wireless Networks and Mobile Applications," NSF CNS-0923479, (Co-PI) $1,800,000, 2009-2013, (with A. Sabharwal (PI), B. Aazhang, E. Knightly, and L. Zhong).
8. "IHCS: Multi-Layer Integrated Resource Management for Mobile Wireless Systems" NSF ECCS-0925942, (PI) $350,000, 2009-2012, (with L. Zhong (Co-PI)).

9. “Development of Context Aware Wireless Networks,” Nokia Corporation, (Co-PI), 320,000 Euro, 2009-2010, (with B. Aazhang (PI)).
10. “Leadership University Program: New Applications for DSPs in Networking and Integrated Wireless Sensors” Texas Instruments, Inc., (Co-PI), $1,000,000, 2008-2010, (C. S. Burrus, B. Aazhang, J. R. Cavallaro, E. W. Knightly, R. G. Baraniuk, M. Orchard).
11. “Unifying Application Specific Processors for Communication Systems,” NSF CCF-0541363, (PI) $218,000, 2006-2010.
12. “MRI: Development of WARPnet - A Platform for Programmable and Observable Deployed Wireless Networks,” NSF CNS-0619767, (Co-PI) $811,863, 2006-2010, (with A. Sabharwal (PI), B. Aazhang, J. P. Frantz, E. Knightly).
13. “CRI: Wireless Open-Access Research Platform (WARP) - A Scalable and Extensible Testbed for High Performance Wireless Systems,” NSF CNS 0551692, (Co-PI) $1,516,000, 2006-2010, (with A. Sabharwal (PI), B. Aazhang, J. P. Frantz, E. Knightly).

Past Research Grants

14. “Scalable Mesh Networks: Algorithms, Protocols, and their Implementation,” Nokia Corporation, (Co-PI), 600,000 Euro, 2006-2008, (with B. Aazhang (PI), A. Sabharwal (Co-PI)).
15. “MRI: Development of a National University Wireless Testbed: Rice Configurable Baseband Architecture,” NSF EIA-0321266 (PI) $374,000, 2003-2006, (with B. Aazhang, J. P. Frantz, A. Sabharhal (Co-PIs), (with O. Takeshita, OSU, D. Goeckel, U.Mass., M. Fitz, UCLA (Collaborators).
16. “VLSI Systems Design Education,” AMD Corporation, (PI), $61,000, 1999-2006.
17. “Research in Wireless Communication Systems,” National Instruments Corporation, (PI), $120,000, 2005-2006.
18. “Leadership University: New Applications for DSP in Multimedia Information Processing, Networking and Wireless Communications: Power Aware Wireless Communications” Texas Instruments, Inc., $1,000,000, 2005-2007, (C. S. Burrus, B. Aazhang, J. R. Cavallaro, E. W. Knightly, R. G. Baraniuk, M. Orchard).
19. “Video Surveillance System Design Utilizing TI DaVinci Technology,” Texas Instruments LU Innovation Fund, $10,000, 2006-2007.
20. “Global Wireless Lab: A Three-Continent Collaboration (India-Finland-USA),” Rice University, (Co-PI), $30,000, 2007, (with A. Sabharwal (PI), Behnaam Aazhang).
21. “Algorithms for Next Generation High Data Rate Wireless Systems,” Nokia Corporation, (Co-PI), $648,000, 2003-2005, (with B. Aazhang (PI), A. Sabharwal (Co-PI).
22. “CISE Research Resources: A Comprehensive Multi-tier Wireless Network Development Platform,” NSF EIA-0224458 (PI), $187,244, 2002-2005, (with J. P. Frantz (Co-PI), A. Sabharwal (Co-PI), E. Knightly (Co-PI), B. Aazhang (Co-PI)).
23. “Leadership University: New Applications of DSPs in Networking, Wireless Communications, and Image Processing,” Texas Instruments, Inc., (Co-PI), $1,000,000, 2002-2004, (with C. S. Burrus (PI), B. Aazhang (Co-PI), E. W. Knightly (Co-PI), R. G. Baraniuk (Co-PI), R. Nowak (Co-PI), M. Orchard (Co-PI)).
24. “A Research Platform for Seamless Wireless Networks supporting Multimedia Applications,” Nokia Corporation and Texas Instruments, Inc., (PI), $555,000, 2002-2004, (with B. Aazhang (Co-PI)).
25. “Signal Processing Algorithms and Architectures for CDMA Systems,” Nokia Corporation, Helsinki, Finland, (Co-PI), $444,528, 2000-2002, (with B. Aazhang (PI)).

26. “Seamless Multi-tier Wireless Networks for Multimedia Applications,” NSF ANI-9979465, (Co-PI), $700,000, 1999-2003, (with B. Aazhang (PI), R.G. Baraniuk (Co-PI), E.W. Knightly (Co-PI), D.S. Wallach (Co-PI)).
27. “Implementation of W-CDMA Networks: Advanced Mobile and Basestation Receiver Prototyping,” Texas TDTP, (PI), $211,148, 2000-2002, (with D.H. Johnson (co-PI)).
28. “Development of a Testbed for Wireless Multiuser Communication Systems,” Nokia Corporation and Texas Instruments, Inc., (PI), $500,781, 1998-2001 (with B. Aazhang (Co-PI)).
29. “Leadership University: New Applications of DSPs in Networking and Integrated Wireless Sensors,” Texas Instruments, Inc., (Co-PI), $1,000,000, 1999-2001, (with C. S. Burrus (PI), B. Aazhang (Co-PI), E. W. Knightly (Co-PI), R. G. Baraniuk (Co-PI)).
30. “Development of a High Speed Wireless LAN,” Nokia Corporation, (Co-PI), $241,622, 1999-2000 (with B. Aazhang (PI), E. Erkip (Co-PI), R.G. Baraniuk (Co-PI)).
31. “Development of Multiuser Transceivers for Wireless CDMA Communications,” Texas Technology Development and Transfer Program. TDTP 003604-044, (Co-PI), $201,336, 1998-1999, (with B. Aazhang (PI)).
32. “A Web-Based Engineering Design Tutor,” A.W. Mellon Foundation, (Co-PI), $570,000, 1998-2000, (with M. Terk (PI), W. Zwaenepoel (Co-PI)).
33. “Development of Monitoring and Diagnostic Methods for Robots Used in Remediation of Waste Sites,” DOE DE-FG07-97ER14830, (PI), $94,944, 1997-1999, (subcontract via Foster-Miller Technologies, Inc., Latham, NY).
34. “Advanced Signal Processing for Multiuser Wireless Communications,” Texas Advanced Technology Program, TATP 003604-049, (Co-PI), $255,000, 1996-1997, (with B. Aazhang (PI)).
35. “Architectures for Multiuser Detection and Channel Estimation in CDMA Communication Systems,” NSF NCR-9506681, (Co-PI), $303,597, 1995-1999, (with B. Aazhang (PI)).
36. “Dynamic Fault Tolerance Methods for Robotics,” NSF IRI-9526363, (Co-PI), $50,000, 1995-1997, (with I. D. Walker (PI)).
37. “Architectures for Multiuser Detection and Channel Estimation in CDMA Communication Systems,” Nokia Corporation, Helsinki, Finland, (Co-PI), $511,785, 1995-1999, (with B. Aazhang (PI)).
38. “Failure Mode Analyses of the Hanford Manipulator,” DOE Westinghouse Hanford Company DE-AC04-94AL850, (Co-PI), $52,743, 1994-1995, (with I. D. Walker, (PI).
39. “Enhanced VLSI Microelectronics Manufacturability using Closed-Loop Photolithographic Simulation,” NSF Materials Synthesis and Processing Initiative DDM-9202639, (PI), $330,000, 1992-1996, (with F. K. Tittel (Co-PI), W. L. Wilson, Jr. (Co-PI)).
40. “Dynamic Fault Reconfigurable Robotic System Architectures,” DOE Sandia National Laboratories Contract #18-4379A, (PI), $309,017, 1991-1996, (with I. D. Walker (Co-PI)).
41. “VLSI CORDIC Parallel Processor Architectures for the SVD,” NSF Research Initiation Award MIP-8909498, (PI), $69,400, 1989-1992.

Proposals Recently Submitted

42. “CI-ADDO-NEW: OASIS: An Open-Access Scalable Imaging System for Emerging Mobile Media Applications,” NSF CRI (PI), (with A. Sabharwal, A. Veeraraghavan).
43. “EAGER: Collaborative Research: Cross-Layer Modeling and Design of Energy-Aware Cognitive Radio Networks,” NSF CNS-EAGER (PI), with M. Juntti, University of Oulu, Finland; Olli Silven, University of Oulu, Finland, Mikko Valkama, Tampere University of Technology, Finland.

Other Support for Research and Education

44. Texas Instruments, Dallas, TX. MSP430 Microcontroller Hardware and Software, 2007-Present.
45. National Instruments, Austin, TX. Programmable FPGA, IF, and RF Hardware and Software, 2003-2007.
46. "Advanced Plotting Systems for VLSI Design and Education," Hewlett-Packard Corporation, $19,000, 2000.
47. "Parallel SVD of Arbitrary Matrices on the CM5," Army High Performance Computing Research Center, Minneapolis, MN. Access to Connection Machine 5, 1992-1995.
48. Texas Instruments, Houston, TX. TMS320 Digital Signal Processing Hardware and Software, 1991-Present.
49. Technology Modeling Associates, Palo Alto, CA. DEPICT Photolithography Simulation Software, 1991-1995.

Courses Taught

- Elec 220, Fundamentals of Computer Engineering
- Elec 422, VLSI Design I
- Elec 423, VLSI Design II
- Elec 437/630, Multi-tier Wireless Networks (team project course)
- Elec 522, Advanced VLSI Design
- Elec 525, Advanced Computer Architecture
- Elec 625, High Performance Processor Design (with J. K. Bennett)
- Elec 693, 694, Advanced Topics Seminars - Computer Systems

Projects Supervised

- Elec 490, Senior Independent Projects
- Elec 491, 492, Senior Honors Projects
- Elec 590, 599, Graduate Independent Projects

Graduate Students and Theses Supervised – 15 Ph.D., 18 M.S.

Johanna Ketonen

Ph.D. June 2012 (Co-Advisor with M. Juntti at University of Oulu, Finland); "Equalization and Channel Estimation Algorithms and Implementations for Cellular MIMO-OFDM Downlink."

Markus Myllylä

Ph.D. June 2011, (Co-Advisor with M. Juntti at University of Oulu, Finland); "Detection Algorithms and Architectures for Wireless Spatial Multiplexing in MIMO–OFDM Systems,"

Current Address: Renesas Mobile Europe, Oulu, Finland.

Yang Sun

Ph.D. January 2011, "Parallel VLSI Architectures for Multi-Gbps MIMO Communication Systems,"

Current Address: Broadcom, Inc., Sunnyvale, CA.

Kiarash Amiri

Ph.D. January 2011, "Cooperative Partial Detection for MIMO Relay Networks"

M.S. May 2007, "Architecture for Detection in MIMO Wireless Systems,"
Current Address: Microsoft, Inc., Redmond, WA.

Marjan Karkooti
Ph.D. May 2009, "Distributed Partial Decoding in Cooperative Communication Systems,"
M.S. May 2004, "Semi-Parallel Architectures For Real-time LDPC Coding,"
Current Address: Patterson and Sheridan, LLC, Houston, TX.

Predrag Radosavljevic
Ph.D. May 2008, "Sphere Detection and LDPC Decoding Algorithms and Architectures for Wireless Systems,"
M.S. May 2004 "Channel Equalization Algorithms for MIMO Downlink and ASIP Architectures,"
Current Address: Patterson and Sheridan, LLC, Houston, TX.

Michael Brogioli,
Ph.D. May 2007, "Reconfigurable Heterogeneous DSP/FPGA Based Embedded Architectures for Numerically Intensive Computing Workloads,"
Current Address: Freescale Semiconductor, Austin, TX.

Yuanbin Guo,
Ph.D. May 2005, "Advanced MIMO-CDMA Receiver for Interference Suppression: Algorithms, System-on-Chip Architectures and Design Methodology,"
Current Address: Huawei, Inc., San Diego, CA.

Sridhar Rajagopal
Ph.D. May 2004, "Data-parallel Digital Signal Processors: Algorithm Mapping, Architecture Scaling and Workload Adaptation,"
M.S. May 2000, "Baseband Architecture Design for Future Wireless Base-Station Receivers,"
Current Address: Samsung, Inc., Dallas, TX.

Martin Leuschen
Ph.D. January 2002, "Derivation and Application of Nonlinear Analytical Redundancy Techniques with Applications to Robotics," (co-supervised with I. D. Walker).
M.S. May 1997, "Robot Reliability Through Fuzzy Markov Models,"
Current Address: ICx Technologies, Oklahoma City, Oklahoma.

Suman Das
Ph.D. September 2000, "Multiuser Information Processing in Wireless Communication," (co-supervised with B. Aazhang).
M.S. May 1997, "Design of Computationally Efficient Multiuser Detectors for CDMA Systems,"
Current Address: Huawei, Inc., New York, New York

Chaitali Sengupta
Honored by MIT Technology Review in Top 100 Young Innovators of 2004
Ph.D. December 1998, "Algorithms and Architectures for Channel Estimation in Wireless CDMA Communication Systems," (co-supervised with B. Aazhang).
M.S. May 1995, "An Integrated CAD Framework Linking VLSI Layout Editors & Process Simulators,"
Current Address: SNR Labs, Corp., Richardson, TX.

Kishore Kota
Ph.D. May 1996, "Parallel Algorithms and Architectures for Near-Far Resistant CDMA Acquisition,"
M.S. May 1991, "Architectural, Numerical and Implementation Issues in the VLSI Design of an Integrated CORDIC-SVD Processor,"
Current Address: Broadcom, Inc., Irvine, CA.

Monica L. Visinsky
Ph.D. May 1994, "Dynamic Fault Detection and Intelligent Fault Tolerance for Robotics," (co-supervised with I. D. Walker)
M.S. December 1991, "Fault Detection and Fault Tolerance Methods for Robotics," (co-supervised with I. D. Walker)
Current Address: Oceaneering Space Systems, Houston, TX.

Nariankadu D. Hemkumar
Ph.D. May 1994, "Efficient VLSI Architectures for Matrix Factorizations,"
M.S. May 1991, "A Systolic VLSI Architecture for Complex SVD,"
Current Address: Cirrus Logic, Austin, TX

Michael Wu
M.S. May 2010, "On the Application of Graphics Processor to Wireless Receiver Design,"
Current Address: Ph.D. Student, Rice University, Houston, TX.

Manik Gadhiok
M.S. January 2007, **"**Architectures for Synchronization in OFDM Wireless Systems,"
Current Address: Virginia Tech, Blacksburg, VA.

Mani Vaya,
M.S. January 2003, "VITURBO: A Reconfigurable Architecture for Ubiquitous Wireless Networks,"
Current Address: Qualcomm, Inc., San Diego, CA.

Vikram Chandrasekhar
M.S., January 2003, "Reducing Dynamic Power Consumption in Next Generation DS-CDMA Mobile Communication Receiver,"
Current Address: Texas Instruments, Dallas, TX

Bryan Jones
M.S. May 2002, "Rapid Prototyping of Wireless Communications Systems,"
Current Address: Mississippi State University, Mississippi State, MS

Kanu Chadha
M.S. May 2001, "A Reconfigurable Decoder Architecture for Wireless LAN and Cellular Systems,"
Current Address: Qualcomm, Inc., San Diego, CA.

Vishwas Sundaramurthy
M.S. May 1999, "A Software Simulation Testbed for CDMA Wireless Communication Systems,"
Current Address: Powerware, Hyderabad, India

Gang Xu
M.S. May 1999, "Implementation Issues of Multiuser Detection in CDMA Communication Systems,"
Current Address: Texas Instruments, Dallas, TX.

Current Graduate Students

Michael Wu *(Ph.D. student); LTE Uplink Receivers and Graphical Processor Architectures for Wireless Systems.*

Bei Yin *(Ph.D. student); Multi-standard Detection Architectures and Network Coding Architectures.*

Guohui Wang *(Ph.D. student); Architectures for Multi-standard Decoding and Graphical Processor Architectures.*

Aida Vosoughi *(Ph.D. student); Architectures for Data Compression for Distributed Antenna Systems*

Other Rice Univ. Thesis Committees - Minor Member, Ph.D.

Deepa Ramachandran, Ph.D. (ECE) (Clark, Chair) 2011	Mohammad Jaber Borran, Ph.D. (ECE) (Aazhang) 2003
Jeffrey A. Sandoval, Ph.D. (CS) (Cooper) 2011	Liang Sun, Ph.D. (ECE) (Clark) 2003
Cherif Salama, Ph.D. (CS) (Taha) 2010	Li Xu, Ph.D. (CS) (Cooper) 2003
Ricardo A. Vargas, Ph.D. (ECE) (Burrus) 2008	Dinesh Rajan, Ph.D. (ECE) (Aazhang) 2002
Nasir Ahmed, Ph.D. (ECE) (Aazhang) 2005	Chu Xiang, Ph.D. (ECE) (Young) 2001
Krishna Kiran Mukkavilli, Ph.D. (ECE) (Aazhang) 2003	Srikrishna Bhashyam, Ph.D. (ECE) (Aazhang) 2001

Parthasarathy Ranganathan, Ph.D. (ECE) (Adve) 2000	Deirdre L. Hamilton, Ph.D., (ECE) (Walker) 1996
Karen D. Alfrey, Ph.D. (ECE) (Clark) 2000	Arati Deo, Ph.D., (ECE) (Walker) 1995
Andrew Sendonaris, Ph.D. (ECE) (Aazhang) 1999	Juan A. Rodriguez, Ph.D., (ECE) (Wilson) 1994
Yile Guo, Ph.D. (ECE) (Aazhang) 1999	William Dawkins, Ph.D., (ECE) (Sinclair) 1993
Myron A. Diftler, Ph.D. (ECE) (Walker) 1997	Richard Murphey, Ph.D., (ECE) (Clark) 1991
Raghavendra K. Madyastha, Ph.D., (ECE) (Aazhang) 1997	

M.S.

Ahmed Elnably, M.S., (ECE) (Varman, Chair) 2012	Feifei Lou, M.S., (ECE) (Sabharwal) 2005
Hui Wang, M.S., (ECE) (Varman) 2011	Chris Steger, M.S., (ECE) (Aazhang) 2004
Ardalan Amiri Sani, M.S., (ECE) (Zhong) 2011	Junhui Qian, M.S., (ECE) (Clark) 2003
Hang Yu, M.S., (ECE) (Zhong) 2011	Nasir Ahmed, M.S., (ECE) (Aazhang) 2002
Justin Fritz, M.S., (ECE) (Aazhang) 2010	Mahsa Memarzadeh, M.S., (ECE) (Aazhang) 2001
Sid Gupta, M.S., (ECE) (Sabharwal) 2009	Ahmad Khoshnevis, M.S., (ECE) (Aazhang) 2001
Christopher Hunter, M.S., (ECE) (Aazhang) 2008	Ozgur Ertug, M.S., (ECE) (Varman) 2000
Melissa Duarte, M.S., (ECE) (Sabharwal) 2007	Tarik Muharemovic, M.S., (ECE) (Aazhang) 2000
Jeffrey A. Sandoval, M.S., (CS) (Cooper) 2007	Krishna Kirin Mukavilli, M.S., (ECE) (Aazhang) 2000
Arthur Nieuwoudt, M.S., (ECE) (Massoud) 2006	Vasileios Balabanos, M.S., (ECE) (Bennett) 2000

Vinay K. Bharadwaj, M.S., (ECE) (Aazhang) 2000	Stephen E. Bensley, M.S., (ECE) (Aazhang) 1994
Damian Dobric, M.S., (ECE) (Bennett) 2000	Juan A. Rodriguez, M.S., (ECE) (Wilson) 1994
Nadeem Ahmed, M.S., (ECE) (Baraniuk) 2000	Jai Tang, M.S., (ECE) (Varman-Sinclair) 1993
Chu Xiang, M.S., (ECE) (Young) 1999	Jay Greenwood, M.S., (ECE) (Bennett) 1992
Dinesh Rajan, M.S., (ECE) (Aazhang) 1999	Deirdre Hamilton, M.S., (ECE) (Bennett-Walker) 1992
Fulong Zhang, M.S., (ECE) (Clark) 1998	Samir Khushalani, M.S., (ECE) (Clark) 1992
Yile Guo, M.S., (ECE) (Young) 1996	Ping Tian, M.S., (ECE) (Clark) 1992
David Chung, M.S., (ECE) (Clark) 1996	Arati Deo, M.S., (ECE) (Walker) 1991
Michael G. McMahon, M.S., (ECE) (Clark) 1995	Vinay Pai, M.S., (ECE) (Varman) 1991
Andrew Sendonaris, M.S., (ECE) (Aazhang) 1995	William Dawkins, M.S., (ECE) (Sinclair) 1990

External Thesis Referee:

Ph.D. thesis opponent, Linköping University, Linköping, Sweden, 2010.
Ph.D. thesis reviewer, Tampere University of Technology, Tampere, Finland, 2009.
Ph.D. thesis reviewer, Indian Institute of Technology, Kharagpur, 2009, 2008, 1994.
Ph.D. thesis opponent, Royal Institute of Technology, (KTH) Stockholm, Sweden, 2000.

University Service

- First Year Mentoring Program, McMurtry Residential College, 2011-Present.
- Engineering School Advance Triad Junior Faculty Mentoring Program, 2010-Present.
- Engineering School Senior Design Committee, 2008-Present.
- Engineering School Curriculum Planning Committee, 2007-Present.
- Engineering School Curriculum Assessment Committee, 2007-Present.
- Engineering School Leadership Committee, 2007-Present.
- Judge, Rice Undergraduate Research Symposium, 2003.
- Faculty Contact, Undergraduate Recruiting, 2003-2003.
- Member, University Committee on Undergraduate Admissions, 1997-1999.
- Member, Faculty Council, 1991-1992.
  Chair of Elections Committee
  Member of Tenure and Ethics Committee
- Engineering Divisional Advisor, Lovett Residential College, 1990-1996.
- Member, University Committee on Undergraduate Teaching, 1990-1991.
- Faculty Associate, Lovett Residential College, 1989-1999.
  Outstanding Associate, 1990-1991, 1991-1992, 1992-1993, 1993-1994, 1994-1995.
- Member, Ken Kennedy Institute, Computer Information Technology Institute, 1989-Present.

Departmental Service

- Director, Center for Multimedia Communications, 2010-Present.
- Associate Department Chair, ECE Department, 2007-Present.
- Chair of Undergraduate Committee, 2007-Present.
- Chair of Visibility Committee, 2005-2007.
- ECE/CS Computer Systems Lab, Member, 2000-Present.
- Associate Director, Center for Multimedia Communications, 1999-2010.
- Affiliates Committee, Chair, 1999-2004.
- Member of Faculty Search Committee, 1999, 2002-2003.
- Member of Computer Committee, 1998-1999.
- Member of Graduate Committee, 1997-2007, 1988-1992.
- Chair of Computer Engineering Area Committee, 1997-1998.
- Member of Corporate Affiliates Committee, 1995-1996.
- Member of Curriculum Committee, 1994-1995.
- Member of Undergraduate Committee, 1994-1996.
- Chair of Library Committee, 1992-1994.
- Chair of Safety Committee, 1990-1991.
- Member of Space Committee, 1989-1990.

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Community Service

- Mentor, Alliance for Graduate Education and the Professoriate (AGEP), Summer 2000.
- Faculty Mentor Program, Spring Independent School District, Spring, TX, 1990.

Professional Activities

Referee for Proposals:

2012, Review Panelist, ECCS Division, ENG, National Science Foundation,
2012, Review Panelist, IIP Division, ENG, National Science Foundation,
2011, Review Panelist, CNS Division, CISE, National Science Foundation,
2003, Committee of Visitors, C-CR Division, CISE, National Science Foundation,
2003, Review Panelist, EIA Division, CISE, National Science Foundation,
2002, Mail Reviewer, C-CR Division, CISE, National Science Foundation,
2002, Review Panelist, C-CR Division, CISE, National Science Foundation,
2001, Site Review Panelist, EIA Division, CISE, National Science Foundation,
2000, Committee of Visitors, C-CR Division, CISE, National Science Foundation,
2000, Review Panelist, EHR Directorate, National Science Foundation,
2000, Reviewer, U.S. Civilian Research and Development Foundation,
2000, Mail Reviewer, INT Division, National Science Foundation,
1999, Review Panelist, EIA Division, CISE, National Science Foundation,
1999, Review Panelist, C-CR Division, CISE, National Science Foundation,
1998, Review Panelist, EIA Division, CISE, National Science Foundation,
1994, 1996, Review Panelist, DMII Division, ENG, National Science Foundation,
1989 - Present, Mail Reviewer, MIPS and C-CR Division, CISE, National Science Foundation.

Conference Leadership and Editorial:

- Program Chair, 2014 IEEE/ACM GLSVLSI, Houston, TX, (May 2014).
- Finance Chair, 2013 Global SIP, Austin, TX (December 2013).
- Invited Session Organizer, "Heterogeneous and Reconfigurable Computing" 2013, 47th Asilomar Conference on Signal, Systems, and Computers, Pacific Grove, CA, (November 2013).
- Technical Area Chair (TAC), 2012, 46th Asilomar Conference on Signal, Systems, and Computers, Pacific Grove, CA, for Area G, Architecture and Implementation.
- Technical Program Committee Member, Session Chair, for Session 9: Iterative Decoding, and Chair, Student Paper Award Committee, 2012 IEEE Workshop on Signal Processing Systems (SIPS), Quebec City, Quebec, Canada, (October 2012)
- Co-Chair, Program Committee, 2012 IEEE/ACM GLSVLSI, Salt Lake City, Utah, (May 2012).
- Guest Editor, 2011 Special Issue on Algorithm and Implementation Aspects of Channel Codes and Iterative Receivers, *EURASIP Journal on Wireless Communications and Networking,* (with A. Burg, C. Studer, H. Meyr).
- Co-Chair, Program Committee, 2011 IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), Santa Monica, CA, (September 2011).
- Co-Chair, VLSI Design Track, 2011 IEEE/ACM GLSVLSI, Lausanne, Switzerland, (May 2011).

- Co-Chair, VLSI Design Track, 2010 IEEE/ACM GLSVLSI, Providence, RI, (May 2010).
- Chair, Student Travel Grants, 2010 IEEE International Symposium on Information Theory, Austin, TX, (June 2010)
- Guest Editor, 2007 Special Issue on Application-specific Systems, Architectures and Processors, *Journal of VLSI Signal Processing Systems,* (with L. Thiele, S. Rajopadhye, T. Noll).
- Guest Editor, 2006 Special Issue on Reconfigurable Radio Technologies in Support of Ubiquitous Seamless Computing, Kluwer J. Mobile Networks and Applications, Volume 11 Issue 6, December 2006, (with P. Demestichas, G. Vivier).
- Co-Chair, Signal Processing for Communications Symposium, 2004 IEEE Global Communications Conference (GLOBECOM), Dallas, TX.
- General Co-Chair, 2004 IEEE 15th International Conference on Application-specific Systems, Architectures and Processors (ASAP), Galveston, TX.
- Co-Chair, Program Committee, 2003 IEEE 14th International Conference on Application-specific Systems, Architectures and Processors (ASAP), The Hague, The Netherlands.
- Area Editor, Hardware and Architecture, *Encyclopedia of Computer Science and Engineering,* Wiley Interscience, 2002-2003 Edition.
- Publicity Chair, 1997 IEEE 13th Symposium on Computer Arithmetic, Asilomar, CA.
- Publicity Chair, 1996 IEEE International Conference on Neural Networks, Washington, DC.
- Guest Editor, 1996 Special Issue on Safety of Robotics Systems, *Reliability Engineering and System Safety,* (with I. D. Walker, K. E. Petersen).
- Guest Co-Editor, 1994 Special Issue on Fault Tolerance in Robotics, *Journal of Computers and Electrical Engineering,* (with I. D. Walker, M. Jamshidi).

Program Technical Committee:

- Program Committee, 2013 Signal Processing for Communications Symposium, 2013 IEEE Global Communications Conference (GLOBECOM), Atlanta, GA.
- Program Committee, 2013 IEEE International Conference on Communications (ICC), Budapest, Hungary.
- Program Committee, 2012 Signal Processing for Communications Symposium, 2012 IEEE Global Communications Conference (GLOBECOM), Anaheim, CA.
- Program Committee, 2012 IEEE 23rd International Conference on Application-specific Systems, Architectures and Processors, Delft, The Netherlands.
- Program Committee, 2012 IEEE Workshop on Signal Processing Systems, Québec City, Canada.
- Program Committee, 2012 IEEE International Conference on Communications (ICC), Ottawa, Canada.
- Review Committee Member, 2012 IEEE International Symposium on Circuits and Systems, (ISCAS), Circuits and Systems for Communications Track, Seoul, Korea.
- Review Committee Member, 2012 IEEE International Conference on Acoustics, Speech, and Signal Processing, (ICASSP), DiSPS Track, Kyoto, Japan.
- Invited Session Organizer, "DSP Architectures for Wireless Communications" 2011, 45th Asilomar Conference on Signal, Systems, and Computers, Pacific Grove, CA.
- Program Committee, 2011 ICASSP Show & Tell Session, Prague, Czech Republic.
- Program Committee, 2011 IEEE International Conference on Communications (ICC), Kyoto, Japan.
- Program Committee, 2011 Signal Processing for Communications Symposium, 2011 IEEE Global Communications Conference (GLOBECOM), Houston, TX.

- Invited Session Organizer, "Session MP6 Communication Processors and Accelerators" 2010, 44th Asilomar Conference on Signal, Systems, and Computers, Pacific Grove, CA.
- Invited Session Co-Organizer (with M. Juntti), 2010 ICASSP, Dallas, TX.
- Program Committee, 2010 IEEE International Conference on Communications (ICC), Cape Town, South Africa.
- Program Committee, 2010 Signal Processing for Communications Symposium, 2010 IEEE Global Communications Conference (GLOBECOM), Miami, FL.
- Invited Session Organizer, "Session TP7 Communication Processors and Accelerators" 2009 43th Asilomar Conference on Signal, Systems, and Computers, Pacific Grove, CA.
- Program Committee, 2009 IEEE International Conference on Communications (ICC), Dresden, Germany.
- Program Committee, 2009 Signal Processing for Communications Symposium, 2009 IEEE Global Communications Conference (GLOBECOM), Honolulu, HI.
- Invited Session Organizer, "Session TA5b Communication Architectures" 2008 42th Asilomar Conference on Signal, Systems, and Computers, Pacific Grove, CA.
- Program Committee, 2008 IEEE International Conference on Communications (ICC), Beijing, China.
- Program Committee, 2008 Signal Processing for Communications Symposium, 2008 IEEE Global Communications Conference (GLOBECOM), New Orleans, LA.
- Invited Session Organizer, "Session WA5a Programmable and Reconfigurable Architectures" 2007 41th Asilomar Conference on Signal, Systems, and Computers, Pacific Grove, CA.
- Program Committee, 2007 IEEE Microelectronics Systems Education Conf., San Diego, CA.
- Program Committee, 2007 IEEE 18th International Conference on Application-specific Systems, Architectures and Processors, Montreal, Canada, (July 2007).
- Program Committee, 2007 IEEE 18th Annual International Symposium on Personal, Indoor and Mobile Radio Communications (PIMRC), Athen, Greece, (September 2007).
- Program Committee, 2007 ACM/IEEE 17th Great Lakes Symposium on VLSI (GLSVLSI), Stresa-Lago Maggiore, Italy, (March 2007).
- Program Committee, 2007 IEEE International Conference on Communications (ICC), Glasgow, Scotland.
- Invited Session Organizer, "Session MA5a DSP Architectures and Implementations" 2006 40th Asilomar Conference on Signal, Systems, and Computers, Pacific Grove, CA.
- Program Committee, 2006 Signal Processing for Communications Symposium, 2006 IEEE Global Communications Conference (GLOBECOM), San Francisco, CA.
- Program Committee, 2006 IEEE 17th International Conference on Application-specific Systems, Architectures and Processors, Steamboat Streams, CO.
- Program Committee, 2006 IEEE 17th Annual International Symposium on Personal, Indoor and Mobile Radio Communications (PIMRC), Helsinki, Finland.
- Program Committee, 2006 IEEE International Conference on Communications (ICC), Istanbul, Turkey.
- Program Committee, 2005 IEEE 16th International Conference on Application-specific Systems, Architectures and Processors, Samos, Greece.
- Program Committee, 2005 IEEE International Conference on Communications (ICC), Seoul, Korea.
- Program Committee, 2005 IEEE Microelectronics Systems Education Conf., Anaheim, CA.
- Invited Session Organizer, "Session TA2a Wireless Implementations" 2004 38th Asilomar Conference on Signal, Systems, and Computers, Pacific Grove, CA.
- Program Committee, 2004 IEEE Signal Processing Systems Conference (SiPS), Austin, TX.
- Program Committee, 2003 IEEE Microelectronic Systems Education Conf., Anaheim, CA.
- Member, IEEE Transactions on VLSI, Editor-in-Chief Search Committee, 2002.

- Program Committee, 2002 IEEE 13th International Conference on Application-specific Systems, Architectures and Processors, San Jose, CA.
- Program Committee, 2001 IEEE Microelectronic Systems Education Conf., Las Vegas, NV.
- Session Organizer, 2001 Texas Instruments DSP Fest, Wireless Applications, Houston, TX.
- Session Chair, 2000 IEEE 12th International Conference on Application-Specific Systems, Architectures and Processors (ASAP), Boston, MA.
- Session Chair, "WA8a-Turbo Codes and Channel Simulation," 1999 33rd Asilomar Conference on Signal, Systems, and Computers, Pacific Grove, CA.
- Program Committee, 1999 IEEE 14th Symposium on Computer Arithmetic, Adelaide, Australia.
- Program Committee, 1999 IEEE Microelectronic Systems Education Conference.
- Program Committee, 1998 SPIE Symposium on Advanced Signal Processing Algorithms, Architectures, and Implementations VIII, San Diego, CA.
- Program Committee, 1997 IEEE International Conference on Computer Design, Austin, TX.
- Program Committee, 1997 IEEE 13th Symposium on Computer Arithmetic, Asilomar, CA.
- Program Committee, 1995 IEEE 12th Symposium on Computer Arithmetic, Bath, UK.
- Session Chair, 1995 IEEE 12th Symposium on Computer Arithmetic, Bath, UK.
- Program Committee, 1994 International Symposium on Robotics and Manufacturing, Maui, HI.
- Program Committee and Session Chair, 1992 SCS International Simulation Technology Conference, Clear Lake, TX.
- Invited Session Co-Organizer, 1992 International Symposium on Robotics and Manufacturing, Sante Fe, NM, (with I. D. Walker).
- Session Chair, 1991 SIAM Conference on Parallel Processing for Scientific Computing, Houston, TX.

Technical Committees:

- Member, IEEE SPS Design and Implementation Technical Committee, 2010-
- Member, IEEE CAS Circuits & Systems for Communications Technical Committee, 2010-
- Affiliate Member, IEEE SPS Design and Implementation Technical Committee, 2009-
- Student Branch Advisor, IEEE Chapter at Rice University, 1990-1994, 2010-Present.
- Chair, IEEE Computer Society Technical Committee on VLSI, 2002-2010.
- Chair, IEEE Houston Section Circuits and Systems Society, 1990-Present.

Referee for Books and Journal Articles:

IEEE Transactions on Signal Processing; IEEE Signal Processing Magazine; Journal of VLSI Signal Processing; Springer Journal of Signal Processing Systems; IEEE Transactions on Computers; IEEE Transactions on VLSI Systems; IEEE Transactions on Parallel and Distributed Systems; IEEE Computer Magazine; IEEE Journal of Solid-State Circuits; IEEE Transactions on Robotics and Automation; SIAM Journal on Matrix Analysis and Applications; Journal of Computers and Electrical Engineering; Journal of Intelligent and Robotic Systems; Society for Computer Simulation Journal; Journal of Robotics and Computer Integrated Manufacturing; Parallel Computing Journal; Journal of Parallel and Distributed Computing; Transactions on Reconfigurable Technology and Systems; Neurocomputing; Cambridge University Press; *Kluwer Academic Press; Springer Press*

Referee for Conference Papers:

IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP); IEEE International Symposium on Circuits and Systems (ISCAS); IEEE Vehicular Technology Conference; IEEE International Symposium on Spread Spectrum Techniques and Applications; IEEE International Conference on Computer Design; International Conference on Application-Specific Array Processors (ASAP); International Conference on Parallel Processing; Hawaii International Conference on System Sciences; IEEE Symposia on Computer Arithmetic.

Consulting

- 2002-, Point of Product Broadcasting Co., Ltd., Houston, TX.
- 2001, Hewlett Packard, Fort Collins, CO.
- 1995-, Nokia Corporation, Irving, TX and Helsinki, Finland.
- 1994, Baker & Botts, L.L.P., Patent Review, Austin, TX.
- 1990, Compaq Computer Corporation, Houston, TX.

Memberships

- Association for Computing Machinery, Member
- Institute of Electrical and Electronics Engineers, Senior Member.

Journal Publications

Submitted:

1. J. Ketonen, M. Juntti, J. Ylioinas, J. R. Cavallaro, "Decision-directed Channel Estimation Implementation for Spectral Efficiency Improvement in Mobile MIMO-OFDM," *Springer Journal of Signal Processing Systems*, (June 2012, Submitted).

To Appear:

2. Y. Sun, J. R. Cavallaro, "VLSI Architecture for Layered Decoding of QC-LDPC Codes with High Circulant-Weight", *IEEE Transactions on VLSI Systems*, (October 2011, Submitted, June 2012, In Revision, August 2012, Accepted, October 2012,Online).

Appeared:

3. B. Yin, J. R. Cavallaro, "LTE uplink MIMO receiver with low complexity interference cancellation," *Springer Analog Integrated Circuits and Signal Processing*, DOI 10.1007/s10470-012-9945-1, pp. 443-450, Volume 73, Number 2, (February 2012, Received, June 2012, Revised, August 2012, Accepted, August 2012, Online, November 2012, Published).

4. M. Wu, C. Dick, Y. Sun, J. R. Cavallaro, "Low complexity scalable MIMO sphere detection through antenna detection reordering," *Springer Analog Integrated Circuits and Signal Processing*, DOI 10.1007/s10470-012-9894-8, (February 2012, Received, May 2012, Revised, June 2012, Accepted, July 2012, Online).

5. Y. Sun, J. R. Cavallaro, "High-Throughput Soft-Output MIMO Detector Based on Path-Preserving Trellis-Search Algorithm," *IEEE Transactions on VLSI Systems*, Volume 20, Number 7, pp. 1235-1247, (July 2012).

6. P. Radosavljevic, K. J. Kim, J. R. Cavallaro, "Parallel Searching based Sphere Detector for MIMO Downlink OFDM Systems," *IEEE Transactions on Signal Processing*, DOI: 10.1109/TSP.2012.2190595, pp. 3240-3252, Volume 60, Number 6, (June 2012).

7. Y. Sun, J. R. Cavallaro, "Trellis-Search Based Soft-Input Soft-Output MIMO Detector: Algorithm and VLSI Architecture," *IEEE Transactions on Signal Processing*, DOI: 10.1109/TSP.2012.2187646, pp. 2617-2627, Volume 60, Number 5 (May 2012).

8. M. Wu, Y. Sun, G. Wang, J. R. Cavallaro, "Implementation of a High Throughput 3GPP Turbo Decoder on GPU," *Springer Journal of Signal Processing Systems*, Special Issue on SiPS 2010, DOI 10.1007/s11265-011-0617-7, (On-Line-First, 10 September 2011), pp. 171-183, Volume 65, Number 2, (November 2011).

9. K. Amiri, M. Wu, J. R. Cavallaro, J. Lilleberg, "Cooperative Partial Detection Using MIMO Relays," *IEEE Transactions on Signal Processing*, pp. 5039-5049, Volume 59, Number 10, (October 2011).

10. Y. Sun, J. R. Cavallaro, "Efficient Hardware Implementation of a Highly-parallel 3GPP LTE/LTE-advance Turbo Decoder" *Elsevier Integration, the VLSI Journal*, Special Issue on Hardware Architectures for Algebra, Cryptology and Number Theory, DOI:10.1016/j.vlsi.2010.07.001, (On-Line, July 2010), pp. 305-315, Volume 44, Number 4, (September 2011).

11. M. Wu, Y. Sun, S. Gupta, J. R. Cavallaro "Implementation of a High Throughput Soft MIMO Detector on GPU," *Springer Journal of Signal Processing Systems*, pp.123-136, Volume 64, Number 1, (July 2011).

12. Y. Sun, J. R. Cavallaro, "A Flexible LDPC/Turbo Decoder Architecture," *Springer Journal of Signal Processing Systems, Special Issue on the 2008 IEEE SiPS Workshop*, DOI: 10.1007/s11265-010-0477-6, (On-Line First, April 2010), pp 1-16, Volume 64, Number 1, (July 2011).

13. M. Myllylä, J. R. Cavallaro, M. Juntti, "Architecture Design and Implementation of the Metric First List Sphere Detector Algorithm," *IEEE Transactions on VLSI Systems*, DOI: 10.1109/TVLSI.2010.2041800, pp. 895-899, Volume 19, Number 5, (May 2011).

14. M. Myllylä, J. R. Cavallaro, M. Juntti, "Implementation Aspects of List Sphere Decoder Algorithms for MIMO-OFDM Systems," *Elsevier J. Signal Processing*, (On-Line, April 2010), pp. 2863-2876, Volume 90, Number 10, (October 2010).

15. J. Ketonen, M. Juntti, J. R. Cavallaro, "Performance – complexity Comparison of Receivers for a LTE MIMO–OFDM System," *IEEE Transactions on Signal Processing*, pp. 3360-3372, Volume 58, Number 6, (June 2010).

16. P. Radosavljevic, Y. Guo, J. R. Cavallaro, "Probabilistically Bounded Soft Sphere Detection for MIMO-OFDM Receivers: Algorithm and System Architecture," *IEEE Journal on Selected Areas in Communications*, pp. 1318-1330, Volume 27, Number. 8, (October 2009).

17. K. Amiri, J. R. Cavallaro, C. Dick, R. Rao, "A High Throughput Configurable SDR Detector for Multi-user MIMO Wireless Systems", *Springer Journal of Signal Processing Systems, Special Issue on Signal Processing for Software Defined Radio Handsets*, (On-Line First, April 2009), pp. 233-245, Volume 62, Number 2, (February 2011).

18. M. Karkooti, P. Radosavljevic, J. R. Cavallaro, "Configurable LDPC Decoder Architecture for Regular and Irregular Codes," *Springer Journal of VLSI Signal Processing Systems for Signal, Image and Video Technology, Special Issue: 20 Years of ASAP*, pp. 73-88, Volume 53, (November 2008).

19. V. Chandrasekhar, F. Livingston, J. R. Cavallaro, "Reducing Dynamic Power Consumption in Next Generation DS-CDMA Mobile Communication Receivers," *International Journal of Embedded Systems*, pp. 128-140, Volume 3, Number 3, (2008).

20. Y. Guo, J. Zhang, D. McCain, J. R. Cavallaro, "Structured Parallel Architecture for Displacement MIMO Kalman Equalizer in CDMA Systems," *IEEE Transactions on Circuits and Systems - II: Express Briefs*, pp. 122-126, Volume 54, No. 2, (February 2007).

21. Y. Guo, D. McCain, J. R. Cavallaro, A. Takach, "Rapid Industrial Prototyping and SoC Design of 3G/4G Wireless Systems Using a HLS Methodology," *EURASIP Journal on Embedded Systems, special issue on Signal Processing with High Complexity: Prototyping and Industrial Design*, pp. 1-25, Volume 2006, Article ID 14952, DOI: 10.1155/ES/2006/14952, (2006).

22. S. Rajagopal, J. R. Cavallaro, "Truncated On-line Arithmetic with Applications to Communication Systems," *IEEE Transactions on Computers*, pp. 1240-1252, Volume 55, No. 10, (October 2006).

23. Y. Guo, J. R. Cavallaro, "A Low Complexity and Low Power SoC Design Architecture for Adaptive MAI Suppression in CDMA Systems," *Journal of VLSI Signal Processing Systems for Signal, Image and Video Technology*, pp. 195-217, Volume 44, No. 3, (September 2006).

24. Y. Guo, J. Zhang, D. McCain, J. R. Cavallaro, "An Efficient Circulant MIMO Equalizer for CDMA Downlink: Algorithm and VLSI Architecture," *EURASIP Journal on Applied Signal Processing, Special Issue on Implementation Aspects and Testbeds for MIMO Systems*, Volume 2006, Article ID 57134, 18 pages, DOI:10.1155/ASP/2006/57134, (2006).

25. S. Das, E. Erkip, J. R. Cavallaro, B. Aazhang, "Low Complexity Iterative Multiuser Detection and Decoding for Real-Time Applications," *IEEE Transactions on Wireless Communications*, pp. 1455-1460, Volume 4, No. 4, (July 2005).

26. M. L. Leuschen, I. D. Walker, J. R. Cavallaro, "Fault Residual Generation via Nonlinear Analytical Redundancy," *IEEE Transactions on Control Systems Technology*, pp. 452-458, Volume 13, No. 3, (May 2005).

27. S. Rajagopal, J. R. Cavallaro, S. Rixner, "Design Space Exploration for Real-Time Embedded Stream Processors," *IEEE Micro*, pp. 54-66, Volume 24, No. 4, (July-August 2004).

28. B. Jones, J. R. Cavallaro, "A Rapid Prototyping Environment for Wireless Communication Embedded Systems," *EURASIP Journal on Applied Signal Processing, Special Issue on: Rapid Prototyping of DSP Systems*, pp. 603-614, Volume 2003, No. 6, (May 2003).

29. J. R. Cavallaro, "Architectures for Heterogeneous Multi-Tier Networks," *Kluwer Journal on Wireless Personal Communications*, pp. 285-296, Volume 22, No. 2, (August 2002).

30. S. Rajagopal, S. Bhashyam, J. R. Cavallaro, B. Aazhang, "Real-Time Algorithms and Architectures for Multiuser Channel Estimation and Detection in Wireless Base-Station Receivers," *IEEE Transactions on Wireless Communications*, pp. 468-479, Volume 1, No. 3, (July 2002).

31. S. Rajagopal, S. Bhashyam, J.R. Cavallaro, B. Aazhang, "Efficient VLSI Architectures for Multiuser Channel Estimation in Wireless Base-station Receivers", *Journal of VLSI Signal Processing: special issue on ASAP*, pp. 143-156, Volume 31, No. 2, (June 2002).

32. G. Xu, S. Rajagopal, J. R. Cavallaro, B. Aazhang, "VLSI Implementation of the Multistage Detector for Next Generation Wideband CDMA Receivers", *Journal of VLSI Signal Processing: special issue on signal processing for wireless communications: algorithms, performance and architecture*, pp. 21-33, Volume 30, No. 1-3, (March 2002).

33. B. Aazhang, J. R. Cavallaro, "Multi-tier Wireless Communications," *Wireless Personal Communications, Special Issue on Future Strategy for the New Millennium Wireless World*, Kluwer, pp. 323-330, Volume 17, (June 2001).

34. C. Sengupta, J. R. Cavallaro, B. Aazhang, "On Multipath Channel Estimation for CDMA Systems Using Multiple Sensors," *IEEE Transactions on Communications*, pp. 543-553, Volume 49, No. 3, (March 2001).

35. M. L. Leuschen, I. D. Walker, J. R. Cavallaro, "Evaluating the Reliability of Prototype Degradable Systems," *Reliability Engineering and System Safety*, pp. 9-20, Volume 72, (2001).

36. C. Sengupta, J. R. Cavallaro, B. Aazhang, "Subspace-based Tracking of Multipath Channel Parameters for CDMA Systems," *European Transactions on Telecommunications*, pp. 439-447, Volume 9, No. 5, (September - October 1998).

37. J. Feinsmith, J. H. Aylor, R. Hodson, B. Courtois, J. R. Cavallaro, J. Hines, C. Pina, M. Smith, D. Bouldin, "What's Next for Microelectronics Education - Editorial" *IEEE Design and Test of Computers*, pp. 95-102, Volume 14, No. 4, (October-December 1997).

38. C. Sengupta, J. R. Cavallaro, W. L. Wilson, Jr., F. K. Tittel, "Automated Evaluation of Critical Features in VLSI Layouts Based on Photolithographic Simulations," *IEEE Transactions on Semiconductor Manufacturing*, pp. 482-494, Volume 10, No. 4, (1997).

39. Z. L. Horvath, M. Erdélyi, G. Szabó, Zs. Bor, F. K. Tittel, J. R. Cavallaro, "Generation of Nearly Nondiffracting Bessel Beams with a Fabry-Perot Interferometer," *Journal of the Optical Society of America A*, pp. 3009-3013, Volume 14, No. 11, (November 1997).

40. M. Erdélyi, Z. L. Horvath, G. Szabó, Zs. Bor, F. K. Tittel, J. R. Cavallaro, M. C. Smayling, "Generation of Diffraction-free Beams for Applications in Optical Microlithography," *Journal of Vacuum Science and Technology B*, pp. 287-292, Volume 15, No. 2, (March/April 1997).

41. K. E. Petersen, I. D. Walker, J. R. Cavallaro, "Safety of Robotic Systems – Guest Editorial," *Reliability Engineering and System Safety*, pp. 223-224, Volume 53, No. 3, (1996).

42. D. Walker, J. R. Cavallaro, "Failure Mode Analysis for a Hazardous Waste Clean-up Manipulator," *Reliability Engineering and System Safety*, pp. 277-290, Volume 53, No. 3, (1996).

43. M. Erdélyi, Zs. Bor, J. R. Cavallaro, G. Szabó, W. L. Wilson, Jr., C. Sengupta, M. C. Smayling, F. K. Tittel, "Enhanced Microlithography Using Combined Phase Shifting and Off-Axis Illumination," *Japanese Journal of Applied Physics*, pp. L1629-L1631, Volume 34, Part 2, No. 12A, (December 1995).

44. M. Kido, G. Szabó, J. R. Cavallaro, W. L. Wilson, Jr., M. C. Smayling, F. K. Tittel, "Submicron Optical Lithography Based on a New Interferometric Phase Shifting Technique," *Japanese Journal of Applied Physics*, pp. 4269-4273, Volume 34, Part 1, No. 8A, (August 1995).

45. M. L. Visinsky, J. R. Cavallaro, I. D. Walker, "A Dynamic Fault Tolerance Framework for Remote Robots," *IEEE Transactions on Robotics and Automation*, pp. 477-490, Volume 11, No. 4, (1995).

46. M. L. Visinsky, J. R. Cavallaro, I. D. Walker, "Robotic Fault Detection and Fault Tolerance: A Survey," *Reliability Engineering and System Safety*, pp. 139-158, Volume 46, No. 2, (1994).

47. N. D. Hemkumar, J. R. Cavallaro, "Redundant and On-Line CORDIC for Unitary Transformations," *IEEE Transactions on Computers*, Special Issue on Computer Arithmetic, pp. 941-954, Volume 43, No. 8, (August 1994).

48. M. L. Visinsky, J. R. Cavallaro, I. D. Walker, "Expert System Framework for Fault Detection and Fault Tolerance in Robotics," *Computers and Electrical Engineering*, pp. 421-435, Volume 20, No. 5, (1994).

49. I.D. Walker, J. R. Cavallaro, "Parallel VLSI Architectures for Real-Time Kinematics of Redundant Robots," *Journal of Intelligent and Robotic Systems: Theory and Applications*, Special Issue on Computational Aspects of Robot Kinematics, pp. 25-43, Volume 9, No. 1, (1994).

50. N. D. Hemkumar, J. R. Cavallaro, "Simulation of Systolic Arrays on the Connection Machine," *SCS Simulation*, Special Issue on High Performance Computing, pp. 151-159, Volume 61, No. 3, (September 1993).

51. K. Kota, J. R. Cavallaro, "Numerical Accuracy and Hardware Tradeoffs for CORDIC Arithmetic for Special-Purpose Processors," *IEEE Transactions on Computers*, pp. 769-779, Volume 42, No. 7, (July 1993).

52. J. R. Cavallaro, F. T. Luk, "CORDIC Arithmetic for an SVD Processor," *Journal of Parallel and Distributed Computing*, pp. 271-290, Volume 5, No. 3, (June 1988).

In Preparation:

53. Y. Sun, G. Wang, J. R. Cavallaro, "Parallel VLSI Architecture for 3GPP LTE/LTE-Advanced Turbo Decoder," *IEEE Transactions on Signal Processing*, (In Preparation).

54. M. Brogioli, P. Radosavljevic, J. R. Cavallaro, "A General Hardware/Software Codesign Methodology For Embedded Signal Processing and Multimedia Workloads," *IEEE Transactions on Circuits and Systems - I: Regular Papers*, (In Preparation).

55. M. Brogioli, J. R. Cavallaro, "RISD: A Retargetable Compiler Infrastructure for Scalable DSP Architectures for Wireless and Multimedia Applications," *IEEE Transactions on Computers*, (In Preparation).

Contributions to Books

1. Y. Sun, K. Amiri, G. Wang, B. Yin, J. R. Cavallaro, T. Ly, "High-Level Design Tools for Complex DSP Applications," (R. Oshana, M. Brogioli, Eds.), in *Elsevier Digital Signal Processing Handbook*, Elsevier, Waltham, MA, pp. 133-155 (2012).

2. K. Amiri, M. Duarte, J. R. Cavallaro, C. Dick, R. Rao, A. Sabharwal, "FPGA in Wireless Communications Applications," (R. Oshana, M. Brogioli, Eds.), *Elsevier Digital Signal Processing Handbook*, Elsevier, Waltham, MA, pp. 75-101 (2012).

3. Y. Sun, K. Amiri, P. Radosavljevic, J. R. Cavallaro, "Application-Specific DSP Accelerators," (S. Bhattacharyya, E. Deprettere, R. Leupers, J. Takala, Eds.), in *Springer Handbook on Signal Processing Systems, 1st Edition*, Springer, New York, NY, pp. 329-362, (2010).

4. Y. Sun, J. R. Cavallaro, Y. Zhu, M. Goel, "Configurable and Scalable Turbo Decoder Architecture for Multiple 4G Wireless Standards" (S. Adibi, A. Mobasher, T. Tofigh, Eds.) in *Fourth-Generation (4G) Wireless Networks: Applications and Innovations*, IGI-Global Press, pp. 622-643, (2010).

5. S. Rajagopal, J. R. Cavallaro, "Communication Processors," (B. W. Wah, Ed.), in *Wiley Encyclopedia of Computer Science and Engineering*, pp. 471-482, (2009).

6. M. L. Leuschen, I. D. Walker, J. R. Cavallaro "Nonlinear Fault Detection for Hydraulic Systems," *Fault Diagnosis and Fault Tolerance for Mechatronic Systems, Recent Advances*, (F. Caccavale and Luigi Villani, Eds.), (Springer Tracts in Advanced Robotics Volume I, (B. Siciliano, O. Khatib, and F. Groen, Series Eds.), Springer-Verlag, Berlin Heidelberg, Germany, pp. 169-191, (2003).

7. M. L. Visinsky, J. R. Cavallaro, I. D. Walker, “Chapter 3: Robotic Fault Tolerance: Algorithms and Architectures,” *Robotics and Remote Systems in Hazardous Environments*, (M. Jamshidi and P. J. Eicker, Eds.), Prentice Hall, Englewood Cliffs, NJ, pp. 53-73, (1993).

Patents

Issued:

1. P. Radosavljevic, M. Karkooti, A. deBaynast, J. R. Cavallaro, “Method, Apparatus, Computer Program Product and Device Providing Semi-Parallel Low Density Parity Check Decoding using a Block Structured Parity Check Matrix,” filed October 24, 2007, US Patent Application Number 20090113276, Published April 30, 2009, U. S. Patent Number 8,219,876, (Issued July 10, 2012)

2. M. Karkooti, G. Charbit, J. Lilleberg, J. Cavallaro. "Distributed Iterative Decoding for Co-operative Diversity,” Provisional patent application. Nokia Corporation Docket No.: NC60051US-P, Harrington & Smith, PC Docket No.: 859.0107.P1(US), filed May 30, 2008, US Patent Application Number 20080298474, Published December 4, 2008, US Patent Number 8,139,512, (Issued March 20, 2012).

3. K. Amiri, C. H. Dick, R. M. Rao, J. R. Cavallaro, “Detecting In-Phase and Quadrature-Phase Amplitudes of MIMO Communications,” US Patent Application Number 20100007565, filed July 10, 2008, Published January 14, 2010, US Patent Number 8,059,761, (Issued November 15, 2011).

4. K. Amiri, C. H. Dick, R. M. Rao, J. R. Cavallaro, “Symbol Detection in a MIMO Communication System,” US Patent Application Number 20100008451, filed July 10, 2008, Published January 14, 2010,.US Patent Number 8,040,981, (Issued October 18, 2011).

5. K. Amiri, R. M. Rao, C. H. Dick, J. R. Cavallaro, “Detector Using Limited Symbol Candidate Generation for MIMO Communication Systems,” filed March 11, 2008, US Patent Application Number 20090232254, Published September 17, 2009, US Patent Number 8,027,404, (Issued September 27, 2011).

6. Y. Guo, D. McCain, J. R. Cavallaro, “System, Apparatus, and Method for Adaptive Weighted Interference Cancellation using Parallel Residue Compensation,” NC40491, filed February 25, 2005, US Patent Application 20060193374, US Patent Number 7,706,430, (Issued April 27, 2010).

7. Y. Guo, J. Zhang, D. McCain, J. R. Cavallaro, “Reduced Parallel and Pipelined High-Order MIMO LMMSE Receiver Architecture,” NC48137, filed November 24, 2004, US Patent Application 20060109891, US Patent Number 7,492,815, (Issued February 17, 2009).

8. Y. Guo, D. McCain, J. R. Cavallaro, “FFT Accelerated Iterative MIMO Equalizer Receiver Architecture,” filed November 24, 2004, US Patent Application 20060109897, US Patent Number 7,483,480, (Issued January 27, 2009).

9. G. Xu, J. R. Cavallaro, B. Aazhang, “VLSI Implementation of the Differencing Multistage Detection in CDMA Communication Systems,” Chinese patent CN1310888T, European Union Patent EP1101290, U.S. Patent Number 6,529,495, (Issued March 4, 2003).

10. G. Szabó, M. Kido, J. R. Cavallaro, F. K. Tittel, “Interferometric Phase Shifting Method for High Resolution Microlithography,” U.S. Patent Number 5,458,999, (Issued October 17, 1995).

Application Published and Pending:

1. P. Radosavljevic, M. Karkooti, A. de Baynast, J. R. Cavallaro, “Method, Apparatus, Computer Program Product and Device Providing Semi-Parallel Low Density Parity Check Decoding using a Block Structured Parity Check Matrix,” Invention Report, (Submitted November 2006), NC55364TW Nokia Code 55364-TW-NP Taiwan Patent Application Number 97141772 Taiwan Patent Application filed 30 Oct 2008, Taiwan Patent 201018094, (Issued May 1, 2010), US Patent Application 20120240003 A1, (Published September 20, 2012, Pending).

2. G. Wang, Y. Sun, J. R. Cavallaro, Y. Guo, “System and Method for Contention-Free Memory Access in an Interleaver,” HW83062306P, US Provisional Patent Application filed December 17, 2010, U. S. Patent Application filed December 16, 2011, U.S. Patent Application 2012/0166742 (Published June 28, 2012, Pending).

3. K. Amiri, M. Wu, J. R. Cavallaro, J. Lilleberg, “Method and Apparatus for Ordered Partial Detection with MIMO Cooperation,” NC71180US, filed March 2, 2010, US Patent Application 20110216693, (Published September 8, 2011, Pending).

4. D. Shamsi, K. Amiri, B. Aazhang, J. R. Cavallaro, J. Lilleberg, “Adaptive Codebook for Beamforming in Limited Feedback MIMO Systems,” filed December 12, 2007, US Patent Application 20110080964, (Published April 7, 2011, Pending).

5. J. Lilleberg, Y. Sun, J. R. Cavallaro, “Methods and Apparatuses for MIMO Detection,” NC73155US, filed October 14, 2010, Continuation-in-Part filed December 2, 2010, US Patent Application 20100303176, (Published December 2, 2010, Pending).

6. K. J. Kim, P. Radosavljevic, J. R. Cavallaro, “QRD-QLD searching based sphere detector for MIMO receiver,” filed December 14, 2007, US Patent Application Number 20090154600, (Published June 18, 2009, Pending).

7. P. Radosavljevic, M. Karkooti, A. deBaynast, J. R. Cavallaro, “Method, Computer Program Product, Apparatus and Device Providing Scalable Structured High Throughput LDPC Decoding,” filed October 24, 2007, US Patent Application Number 20090113256, (Published April 30, 2009, Pending).

8. Y. Guo, J. Zhang, D. McCain, J. R. Cavallaro, “MIMO Kalman Equalizer for CDMA Wireless Communication,” filed January 4, 2005, US Patent Application Number 20060146759, (Published July 6, 2006, Pending).

Application Pending:

1. B. Yin, K. Amiri, J. R. Cavallaro, Y. Guo, “Method and Device for Interchip and Interantenna Interference Cancellation,” HW83139402P, US Provisional Patent Application filed February 28, 2011, Pending.

2. K. Amiri, J. R. Cavallaro, J. Lilleberg, "Apparatus and Methodology for Cooperative Partial Detection Using MIMO Relays," NC64914 (Submitted May 2008) US Patent Application filed 5 August 2008, Pending.

3. P. Radosavljevic, Y. Guo, J. R. Cavallaro, "Methods and Apparatus for Iterative Detection/Decoding in MIMO-OFDM and SC-OFDMA Systems," Invention Report, (Submitted December 2006).

Invited Conference Presentations

1. Y. Sun, G. Wang, and J. R. Cavallaro, "Multi-Layer Parallel Decoding Algorithm and VLSI Architecture for Quasi-Cyclic LDPC Codes," IEEE ISCAS Special Session on VLSI Architectures for LDPC coding/decoding, pp. 1776-1779, Rio de Janeiro, Brazil, (May 2011).

2. O. Gustafsson, K. Amiri, D. Andersson, A. Blad, C. Bonnet, J. R. Cavallaro, J. Declerck, A. Dejonghe, P. Eliardsson, M. Glasse, A. Hayar, L. Hollevoet, C. Hunter, M. Joshi, F. Kaltenberger, R. Knopp, K. Le, Z. Miljanic, P. Murphy, F. Naessens, N. Nikaein, D. Nussbaum, R. Pacalet, P. Raghavan, A. Sabharwal, O. Sarode, P. Spasojevic, Y. Sun, H. M. Tullberg, T. Vander Aa, L. Van der Perre, M. Wetterwald, and M. Wu, "Architectures for Cognitive Radio Testbeds and Demonstrators – An Overview," Invited Special Session, *2010 5th International Conference on Cognitive Radio Oriented Wireless Networks and Communications (CROWNCOM)*, Cannes, France, (June 2010).

3. P. Radosavljevic, M. Karkooti, A. deBaynast, J. R. Cavallaro, "High-Throughput Multi-Rate LDPC Decoder Based On Architecture-Oriented Parity Check Matrices," *14th European Signal Processing Conference*, Firenze, Italy, (September 2006).

4. J. R. Cavallaro, "VLSI Architectures and Rapid Prototyping Testbeds for Wireless Systems," *International Workshop on Convergent Technologies (IWCT)*, Oulu, Finland, (June 2005).

5. S. Rajagopal, S. Rixner, J. R. Cavallaro, "A Programmable Baseband Processor Design for Software Defined Radios", *IEEE Midwest Conference on Circuits and Systems,* pp. 413-416, Tulsa, OK, (August 2002).

6. S. Das, S. Rajagopal, C. Sengupta, J. R. Cavallaro, "Arithmetic Acceleration Techniques for Wireless Communication Receivers," *33rd IEEE Asilomar Conference on Signal, Systems, and Computers*, pp. 1469-1474, Pacific Grove, CA (October 1999).

7. G. Xu, J. R. Cavallaro, "Real-Time Implementation of the Multistage Algorithm for Next-Generation Wideband CDMA Systems," *Proc. SPIE Conference on Advanced Signal Processing Algorithms, Architectures, and Implementations IX*, Volume 3807, pp. 62-73, Denver, CO (July 1999).

8. M. L Leuschen, J. R. Cavallaro, I. D. Walker, "Monitoring and Diagnostics for a Hydraulic Robot in Hazardous Environments," *Proc. Eighth ANS Topical Meeting on Robotics and Remote Systems*, Pittsburgh, PA (April 1999).

9. B. Haller, J. Götze, J. R. Cavallaro, "Efficient Implementation of Rotation Operations for High-Performance QRD-RLS Filtering," *Proc. IEEE International Conference on*

Application-specific Systems, Architectures, and Processors, (ASAP), pp. 162-174, Zurich, Switzerland (July 1997), Awarded Best Paper Award.

10. J. R. Cavallaro, I. D. Walker, "Failure Mode Analysis of a Proposed Manipulator-based Hazardous Material Retrieval System," *Proc. American Nuclear Society 7th Topical Meeting on Robotics and Remote Systems*, Vol. 2, pp. 1096-1102, Augusta, GA (April 1997).

11. J. R. Cavallaro, C. Sengupta, F. K. Tittel, W. L. Wilson, Jr., "Automated Evaluation of Critical Features in VLSI Layouts Based on Photolithographic Simulations," *Proc. of the NSF Design and Manufacturing Grantees Conference*, SME Press, pp. 345-346, Albuquerque, NM (January 1996).

12. J. R. Cavallaro, F. K. Tittel, W. L. Wilson, Jr., "Submicron Optical Microlithography Based on Interferometric Phase Shifting," *Proc. of the NSF Design, Manufacturing and Industrial Innovation Grantees Conference*, SME Press, pp. 395-396, San Diego, CA (January 1995).

13. D. L. Hamilton, M. L. Visinsky, J. K. Bennett, J. R. Cavallaro, I. D. Walker, "Fault Tolerant Algorithms and Architectures for Robotics," *Proc. IEEE Mediterranean Electrotechnical Conference*, pp. 1034-1036, Antalya, Turkey (April 1994).

14. J. R. Cavallaro, I. D. Walker, "A Survey of NASA and Military Standards on Fault Tolerance and Reliability Applied to Robotics," *Proc. AIAA/NASA Conference on Intelligent Robots in Field, Factory, Service, and Space (CIRFFSS'94)*, pp. 282-286, Houston, TX (March 1994).

15. H. M. Fossati, F. K. Tittel, W. L. Wilson, J. R. Cavallaro, "Enhanced VLSI Manufacturability using an Integrated CAD Framework," *Proc. of the NSF Design and Manufacturing Grantees Conference*, SME Press, pp. 549-550, Boston, MA (January 1994).

16. M. Kido, J. R. Cavallaro, G. Szabó, W. L. Wilson, F. K. Tittel, "A New Phase Shifting Method for High Resolution Microlithography," *Proc. of the NSF Design and Manufacturing Grantees Conference*, SME Press, pp. 577-578, Boston, MA (January 1994).

17. M. L. Visinsky, J. R. Cavallaro, I. D. Walker, "Expert System Framework of Fault Detection and Fault Tolerance for Robots," *Proc. Fourth International Symposium on Robotics and Manufacturing*, ASME Press Series on Robotics and Manufacturing, Volume 4, pp. 793-799, Sante Fe, NM (November 1992).

Invited Lectures, Tutorials, Short Courses and Visits

1. Invited Lecture, "FPGA-based wireless communications**"** IEEE Signal Processing Society's High Performance DSP and FPGA implementation of Signal Processing Systems Summer School 2012, Queen's University Belfast (QUB), Belfast, Northern Ireland, (August 20-24, 2012).

2. Keynote Presentation, "WARP - A Testbed for Wireless Algorithm Design and Experimentation: The Rice University Wireless Open-Access Research Platform," 8th Workshop on Optimizations for DSP and Embedded Systems (ODES-8), in conjunction with IEEE/ACM International Symposium on Code Generation and Optimization (CGO), Toronto, Canada, (April 25, 2010).

3. Panelist, “Programming High Performance Signal Processing Systems in High Level Languages,” 18th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, Monterey, CA, (February 22, 2010).

4. M. Juntti, J. R. Cavallaro, “Tutorial on Signal Processing in Wireless Systems,” International Symposium on System-On-Chip Tutorial, Tampere, Finland, (October 5, 2009).

5. Short Course, “Topics in Wireless Systems Architecture,” Center for Wireless Communication, University of Oulu, Finland, (August 17-18, 2009)

6. M. Juntti, J. R. Cavallaro, “Baseband Algorithms and Architectures for Cooperative MIMO Systems with Applications to Evolving System Standards,” IEEE Wireless VITAE Tutorial, Aalborg, Denmark, (May17, 2009).

7. M. Juntti, J. R. Cavallaro, “Baseband Algorithms and Architectures for Cooperative MIMO Systems with Applications to Evolving System Standards,” 2009 WCNC Tutorial, Budapest, Hungary, (April 5, 2009).

8. “Algorithm and Architecture Design and Evaluation on the Rice University Wireless Open-Access Research Platform (WARP)”, Univ. of Texas, Dallas, Electrical Engineering Seminar Series & Dallas Chapter of IEEE Signal Processing Society, Dallas, TX, (November 17, 2008).

9. “M. Juntti, J. R. Cavallaro, “MIMO Baseband Algorithms & Architectures with Applications to 3G LTE & WiMAX Systems,” IEEE Intl. Symposium on Circuits and Systems (ISCAS) Tutorial, Seattle, WA, (May 18, 2008).

10. “Algorithm and Architecture Design and Evaluation on the Rice University Wireless Open-Access Research Platform,” IEEE Galveston Bay Section, NASA JSC, Houston, TX, (March 28, 2008).

11. “Algorithm and Architecture Design on the Rice Univ. Wireless Open-Access Research Platform (WARP),” IEEE Globecom Design and Developers Forum Panel on Current and Future Trends in Software Designed Radio/Cognitive Radio (SDR/CR) Design & Development, Washington, DC, (November 28, 2007).

12. “A Software Simulation Testbed for Third Generation CDMA Wireless Systems,” National Instruments NI-Week, Austin, TX (August 17, 2005).

13. “Architectures, Algorithms, and Research Platforms for Wireless Communication,” Nokia Research Center, Helsinki, Finland (June 3, 2005).

14. “Architectures, Algorithms, and Research Platforms for Wireless Communication,” Tampere Univ. of Technology, Finland (May 2x, 2005).

15. “A Software Simulation Testbed for Third Generation CDMA Wireless Systems,” National Instruments NI-Week, Austin, TX (August 17, 2004).

16. “Architectures, Algorithms, and Research Platforms for Wireless Communication,” Univ. of Oulu, Finland (June 15, 2004).

17. “Advanced Algorithms, Architectures, and Implementations for W-CDMA and WLAN Communication Systems,” (Short Course with B. Aazhang), Univ. of Oulu, Finland (August 12-14, 2002).

18. “Reconfigurable VLSI Communication Processor Architectures” Workshop on Future Wireless Communication Systems and Algorithms, University of Oulu, Oulu, Finland (August 12, 2002).

19. “Architectures for Heterogeneous Multi-tier Wireless Networks,” Panelist, Third Strategic Workshop on Wireless Communications, Rebild, Denmark (September 9, 2001).

20. “Scheduling of Advanced Communication Receiver Algorithms on Custom VLSI Architectures,” Hewlett Packard VLSI Laboratory, Fort Collins, CO (July 19, 2001).

21. “VLSI Architectures for Multi-tier Wireless Networks,” Hewlett Packard VLSI Laboratory, Fort Collins, CO (July 18, 2001).

22. “Rice Everywhere Network (RENE)” University of Oulu, Oulu, Finland (June 15, 2001).

23. “VLSI Architectures for Multi-tier Wireless Systems.” University of Queensland, Brisbane, Australia (May 14, 2001).

24. “VLSI Architectures for Multi-tier Wireless Systems,” Lulea University of Technology, Lulea, Sweden (August 20, 2000).

25. “VLSI Architectures for Multi-tier Wireless Systems,” University of Michigan, EECS Dept., Ann Arbor, MI (November 9, 1999).

26. “Overview of Implementation Issues for Multi-tier Networks on DSPs,” Berkeley Wireless Research Center, Berkeley, CA (October 22, 1999).

27. “Overview of Implementation Issues for Multi-tier Networks on DSPs,” KTH Royal Institute of Technology, Stockholm, Sweden (August 19, 1999).

28. “Overview of Implementation Issues for Multi-tier Networks on DSPs,” Helsinki University of Technology, Helsinki, Finland, (August 18, 1999).

29. “Overview of Implementation Issues for Multi-tier Networks on DSPs,” University of Oulu, Oulu, Finland (August 16, 1999).

30. “Multiuser Techniques for Channel Estimation and Detection for CDMA Systems,” Texas Instruments TMS320 Educators Conference, Houston, TX (with C. Sengupta, J. R. Cavallaro, B. Aazhang, et al., August 1998).

31. “Architectures and Signal Processing Algorithms for CDMA Communications,” Nokia Corporation, San Diego, CA (Short Course with B. Aazhang, September 26-27, 1996).

32. “Architectures and Signal Processing Algorithms for CDMA Communications,” Nokia Research Center, Helsinki, Finland (Short Course with B. Aazhang, August 28-29, 1996).

33. "Parallel VLSI/DSP Architectures for CDMA Communication Systems," Department of Electrical Engineering, Swiss Federal Institute of Technology (ETH), Zürich, Switzerland (July 18, 1995).

34. "VLSI CORDIC Co-Processors for DSP," Texas Instruments, Houston, TX (January 26, 1993).

35. "CORDIC Parallel Processor Architectures for an SVD Processor," IBM Almaden Research Center, San Jose, CA (July 21, 1989).

36. "CORDIC Algorithms for Digital Signal Processing," Texas Instruments, Houston, TX (July 7, 1989).

37. "VLSI Implementation of a CORDIC SVD Processor," Mitre Corporation, Bedford, MA (June 14, 1989).

Reviewed Conference Publications - From Full Paper

1. G. Wang, Y. Xiong, J. Yun, and J. R. Cavallaro, "Accelerating Computer Vision Algorithms Using Opencl Framework on Mobile Devices - A Case Study," *2013 IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, May 26-31, 2013, Vancouver, Canada (December 2012, Submitted).

2. Yin, M. Wu, C. Studer, J. R. Cavallaro, and C. Dick, "Implementation Trade-Offs For Linear Detection In Large-Scale Mimo Systems," *2013 IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, May 26-31, 2013, Vancouver, Canada (December 2012, Submitted).

3. Rister, G. Wang, M. Wu and J. R. Cavallaro, "A Fast and Efficient Sift Detector Using The Mobile Gpu," *2013 IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, May 26-31, 2013, Vancouver, Canada (December 2012, Submitted).

4. G. Wang, A. Vosoughi, H. Shen, J. R. Cavallaro and Y. Guo, "Parallel Interleaver Architecture with New Scheduling Scheme for High Throughput Configurable Turbo Decoder," *IEEE International Symposium on Circuits and Systems (ISCAS 2013)*, Beijing, China, May 2013 (October 2012, Submitted, December 2012, Accepted).

5. M. Wu, B. Yin, A. Vosoughi, C. Studer, J. R. Cavallaro and C. Dick, "Approximate Matrix Inversion for High-Throughput Data Detection in Large-Scale MIMO Uplink, " *IEEE International Symposium on Circuits and Systems (ISCAS 2013)*, Beijing, China, May 2013 (October 2012, Submitted, December 2012, Accepted).

6. A. Vosoughi, M. Wu, and J. R. Cavallaro, "Baseband Signal Compression in Wireless Base Stations," *IEEE Global Communications Conference (GLOBECOM)*, Anaheim, CA, December 2012, (March 2012, Submitted, July 2012, Accepted).

7. M. Wu, B. Yin, and J. R. Cavallaro, "Flexible N-Way MIMO Detector on GPU," *IEEE Workshop on Signal Processing Systems (SiPS 2012)*, pp. 318-323, Québec City, Québec, Canada, October 2012, (June 2012, Accepted), (October 2012).

8. B. Yin, K. Amiri, J. R. Cavallaro, and Y. Guo, "Reconfigurable Multi-Standard Uplink MIMO Receiver with Partial Interference Cancellation," *IEEE International Conference on Communications (ICC)*, pp. 6282-6286, Ottawa, Canada, (Submitted, September 2011, Accepted, January 2012), (June 2012).

9. M. Wu, C. Dick, J. R. Cavallaro, "Improving MIMO Sphere Detection Through Antenna Detection Order Scheduling," *Software Defined Radio Forum 2011*, pp. 280-284, Washington, DC, (November-December 2011), (Accepted, August 2011) (June 2012).

10. B. Yin, J. R. Cavallaro, "Low complexity MMSE based interference cancellation for LTE uplink MIMO receiver," *Software Defined Radio Forum 2011*, pp. 18-22, Washington, DC, (November-December 2011), (Accepted, August 2011) (June 2012).

11. G. Wang, M. Wu, Y. Sun, J. R. Cavallaro, "High-Throughput Contention-Free Concurrent Interleaver Architecture for Multi-Standard Turbo Decoder," *IEEE International Conference on Application-specific System, Architectures and Processors (ASAP'11)*, pp. 113-121, Santa Monica, CA (Accepted, June 2011),(September 2011)

12. G. Wang, M. Wu, Y. Sun, J. R. Cavallaro, "A Massively Parallel Implementation of QC-LDPC Decoder on GPU," IEEE Symposium on Application Specific Processors (SASP), pp. 82-85, San Diego, CA, (June 2011).

13. K. Amiri, C. Dick, R. Rao, J. R. Cavallaro, "Reduced Complexity Soft MMSE MIMO Detector Architecture," *Software Defined Radio Forum 2010*, (***Outstanding Paper Award***), pp. 716-720, Washington, DC, (November-December 2010).

14. M. Wu, Y. Sun, J. R. Cavallaro, "Implementation of a 3GPP LTE Turbo Decoder Accelerator on GPU," *IEEE Workshop on Signal Processing Systems (SiPS)*, pp. 192-197, San Francisco, CA, (October 2010).

15. K. Amiri, M. Wu, M. Duarte, J. R. Cavallaro, "Physical Layer Algorithm and Hardware Verification of MIMO Relays Using Cooperative Partial Detection," *IEEE ICASSP*, pp. 5614-5617, Dallas, TX, (March 2010).

16. Y. Sun, J. R. Cavallaro, "Low-Complexity and High-Performance Soft MIMO Detection Based on Distributed M-Algorithm through Trellis-Diagram," *IEEE ICASSP*, pp. 3398-3401, Dallas, TX, (March 2010).

17. M. Wu, S. Gupta, Y. Sun, J. R. Cavallaro, "A GPU Implementation of a Real-Time MIMO Detector," *IEEE Workshop on Signal Processing Systems (SiPS)*, pp. 303-308, Tampere, Finland, (October 2009).

18. Y. Sun, J. R. Cavallaro, T. Ly, "Scalable and Low Power LDPC Decoder Design Using High Level Algorithmic Synthesis," *22nd IEEE International SOC Conference*, pp. 267-270, Belfast, Northern Ireland, (September 2009).

19. Y. Sun, J. R. Cavallaro, "High Throughput VLSI Architecture for Soft-Output MIMO Detection Based on a Greedy Graph Algorithm", *ACM/IEEE Great Lakes Symposium on VLSI*, (***Best Student Paper Award***), pp. 445-450, Boston, MA, (May 2009).

20. M. Myllylä, M. Juntti, J. R. Cavallaro "Architecture Design and Implementation of the Increasing Radius - List Sphere Detector Algorithm," *IEEE ICASSP*, pp. 553.556, Taipei, Taiwan, (April 2009).

21. K. Amiri, J. R. Cavallaro, "Partial Detection for Multiple Antenna Cooperation", CISS, pp. 669-674, Baltimore, MD, (March 2009).

22. K. Amiri, C. Dick, R. Rao, J. R. Cavallaro, "Novel Sort-Free Detector with Modified Real-valued Decomposition Ordering in MIMO Systems," *IEEE Global Communications Conference (GLOBECOM)*, pp. 1-5, New Orleans, LA, (Nov.-Dec. 2008).

23. P. Radosavljevic, K. J. Kim, J. R. Cavallaro, "QRD-QLD searching based sphere detection for emerging MIMO downlink OFDM receivers", *IEEE Global Communications Conference (GLOBECOM)*, pp. 1-5, New Orleans, LA, (Nov.-Dec. 2008).

24. K. Amiri, C. Dick, R. Rao, J. R. Cavallaro, "Flex-Sphere: An FPGA Configurable Sort-Free Sphere Detector for Multi-user MIMO Wireless Systems," *Software Defined Radio Forum 2008*, Washington, DC, (October 2008).

25. Y. Sun, J. R. Cavallaro, "Unified Decoder Architecture for LDPC/Turbo Codes," *2008 IEEE Workshop on Signal Processing Systems, (SiPS)*, pp. 13-18, Washington, DC, (***Awarded "Bob Owens Memorial Paper Award."***), (October 2008).

26. Y. Sun, J. R. Cavallaro, "A Low Power 1-Gbps Reconfigurable LDPC Decoder Design for Multiple 4G Wireless Standards," *IEEE International SoC Conference (SOCC'08)*, pp. 367-370, Newport Beach, CA, (***Best Paper Award***), (September 2008).

27. M. Myllylä, M. Juntti, J. R. Cavallaro, "The Effect of Preprocessing to the Complexity of List Sphere Detector Algorithms," *2008 WPMC*, Lapland, Finland, (September 2008).

28. Y. Sun, Y. Zhu, M. Goel, J. R. Cavallaro, "Configurable and Scalable High Throughput Turbo Decoder Architecture for Multiple 4G Wireless Standards," *IEEE International Conference on Application-specific System, Architectures and Processors (ASAP'08)*, pp. 209-214, Leuven, Belgium (July 2008).

29. K. Amiri, Y. Sun, P. Murphy, C. Hunter, J. R. Cavallaro, A. Sabharwal, "WARP, a Unified Wireless Network Testbed for Education and Research," *IEEE International Conference on Microelectronic Systems Education (MSE)*, pp. 53-54, San Diego, CA, (June 2007).

30. Y. Sun, M. Karkooti, J. R. Cavallaro, "VLSI Decoder Architecture for High Throughput,Variable Block-size and Multi-rate LDPC Codes," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2104-2107, New Orleans, LA, (May 2007).

31. M. Karkooti, P. Radosavljevic, J. R. Cavallaro, "Configurable, High Throughput, Irregular LDPC Decoder Architecture: Tradeoff Analysis and Implementation," *Proc. IEEE 17th International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, pp. 360-367, Steamboat Springs, CO (September 2006).

32. P. Radosavljevic, A. de Baynast, M. Karkooti, J. R. Cavallaro, "Multi-Rate High-Throughput LDPC Decoder: Tradeoff Analysis Between Decoding Throughput and Area," *Proc. 17th Annual IEEE International Symposium on Personal, Indoor and Mobile Radio*

Communications (PIMRC'06), DOI: 10.1109/PIMRC.2006.254392, Helsinki, Finland, (September 2006).

33. M. Myllylä, P. Silvola, M. Juntti, J. R. Cavallaro, "Comparison of Two Novel List Sphere Detector Algorithms For MIMO-OFDM Systems," *Proc. 17th Annual IEEE International Symposium on Personal, Indoor and Mobile Radio Communications (PIMRC'06),* DOI: 10.1109/PIMRC.2006.254384, Helsinki, Finland, (September 2006).

34. M. Brogioli, P. Radosavljevic, J. R. Cavallaro, "Hardware/Software Co-design Methodology for DSP/FPGA Partitioning: A Case Study for Meeting Real-Time Processing Deadlines in 3.5G Mobile Receivers," *Proc. 49th IEEE International Midwest Symposium on Circuits and Systems*, San Juan, PR, (August 2006).

35. Y. Guo, J. Zhang, D. McCain, J. R. Cavallaro, "Displacement MIMO Kalman Equalizer for CDMA Downlink in Fast Fading Channels," *Proc. IEEE GLOBECOM,* pp. 2281-2286, St. Louis, MO, (November 2005).

36. M. Gadhiok, R. Hardy, P. Murphy, P. Frantz, H. Choi, J. R. Cavallaro, "An FPGA-based Daughtercard for TI's C6000 family of DSKs," *Proc. IEEE International Conference on Microelectronic Systems Education (MSE),* pp. 85-86, Anaheim, CA, (June 2005).

37. Y. Guo, D. McCain, J. R. Cavallaro, "FFT-Accelerated Iterative MIMO Chip Equalizer Architecture for CDMA Downlink," *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP),* Volume 3, pp. 1005-1008, Philadelphia, PA (March 2005).

38. S. Rajagopal, S. Rixner, J. R. Cavallaro, "Improving Power Efficiency in Stream Processors Through Dynamic Cluster Reconfiguration," *6th Workshop on Media and Streaming Processors*, Portland, OR, (December 2004).

39. Y. Guo, J. Zhang, D. McCain, J. R. Cavallaro, "Efficient MIMO Equalization for Downlink Multi-Code CDMA: Complexity Optimization and Comparative Study," *Proc. IEEE GLOBECOM*, Volume 4, pp. 2513 - 2519, Dallas, TX, (November 2004).

40. de Baynast, P. Radosavljevic, J. R. Cavallaro, "Chip level LMMSE Equalization for Downlink MIMO CDMA in Fast Fading Environments," *Proc. IEEE GLOBECOM*, Volume 4, pp. 2552-2556, Dallas, TX, (November 2004).

41. Y. Guo, D. McCain, J. R. Cavallaro, "Low Complexity System-On-Chip Architectures of Optimal Parallel-Residue-Compensation In CDMA Systems," *Proc. IEEE International Symposium on Circuits and Systems (ISCAS),* pp. 77-80, Volume 4, Vancouver, Canada (May 2004).

42. M. Karkooti, J. Cavallaro, "Semi-parallel Reconfigurable Architectures for Real-time LDPC Decoding," *Proc. IEEE International Conference on Information Technology (ITCC),* pp. 579-585, Volume 1, Las Vegas, NV (April 2004).

43. V. Chandrasekhar, F. Livingston, J. R. Cavallaro, "Reducing Dynamic Power Consumption in Next Generation DS-CDMA Mobile Communication Receivers," *Proc. IEEE 14th International Conference on Application-specific Systems, Architectures and Processors (ASAP),* pp. 251-261, The Hague, The Netherlands (June 2003).

44. Y. Guo, G. Xu, D. McCain, J. R. Cavallaro, "Rapid Scheduling of Efficient FPGA Architectures for Next-Generation HSDPA Wireless System Using Precision C Synthesizer," *Proc. 14th IEEE International Workshop on Rapid Systems Prototyping (RSP 2003)*, pp. 179-185, San Diego, CA, (June 2003).

45. P. Murphy; J. P. Frantz, E. Welsh; R. Hardy, T. Mohsenin, J. R. Cavallaro, "VALID: Custom ASIC Verification and FPGA Education Platform" *Proc. 2003 IEEE International Conference on Microelectronic Systems Education*, pp. 66-67, Anaheim, CA, (June 2003).

46. J. R. Cavallaro, M. Vaya, "VITURBO: A Reconfigurable Architecture for Viterbi and Turbo Decoding," *Proc. IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, pp. 497-500, Volume II, Hong Kong, China (April 2003).

47. Y. Guo, J. R. Cavallaro, "Enhanced Power Efficiency of Mobile OFDM Radio using Predistortion and Post-Compensation," *Proc. IEEE 56th Vehicular Technology Conference*, pp. 214-218, Vancouver, BC, Canada (September 2002).

48. M. L. Leuschen, I. D. Walker, J. R. Cavallaro, "Nonlinear Fault Detection for Hydraulics: Recent Advances in Fault Diagnosis and Fault Tolerance for Mechatronic Systems," in Proc. 17th IEEE International Symposium on Intelligent Control, Vancouver, BC, Canada (October 2002).

49. Y. Guo, J. R. Cavallaro, "Post-Compensation Of RF Non-Linearity In Mobile OFDM Systems By Estimation Of Memory-Less Polynomial, *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 217-220, Volume I, Scottsdale, AZ (May 2002).

50. F. Livingston, V. Chandrasekhar, M. Vaya, J. R. Cavallaro, "Handset Detector Architectures for DS-CDMA Wireless Systems", *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 265-268, Volume III, Scottsdale, AZ (May 2002).

51. Y. Guo, J. R. Cavallaro, "A Novel Adaptive Pre-Distorter Using LS Estimation Of SSPA Non-Linearity In Mobile OFDM Systems", *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 453-456, Volume III, Scottsdale, AZ (May 2002).

52. M. L. Leuschen, J. R. Cavallaro, I. D. Walker, "Robotic Fault Detection Using Nonlinear Analytical Redundancy", *Proc. IEEE International Conference on Robotics and Automation*, pp. 456-463, Washington, DC (May 2002).

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Reviewed Conference Publications - From Extended Abstract

1. S. Su, J. Kerwin, S. Crowe, J. R. Cavallaro and G. L. Woods, "Teaching Embedded Programming to Electrical Engineers, BioEngineers, and Mechanical Engineers via the Escape Platform," *3rd Interdisciplinary Engineering Design Education Conference (IEDEC 2013)* Santa Clara, CA, March 2013, (October 2012, Submitted, December 2012, Accepted)

2. S. C. Kim, W. L. Plishker, S. S. Bhattacharyya and Joseph R. Cavallaro, "GPU-Based Acceleration of Symbol Timing Recovery," *Conference on Design & Architectures for Signal & Image Processing (DASIP 2012),* Karlsruhe, Germany, (October 2012) (June 2012, Accepted, December 2012, Published)).

3. J. Ketonen, M. Juntti, J. Ylioinas, and J. R. Cavallaro, "Implementation of LS, MMSE and SAGE Channel Estimators for Mobile MIMO-OFDM," *2012 IEEE Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, CA, November 2012, (May 2012, Submitted, June 2012, Accepted).

4. G. Wang, H. Shen, B. Yin, Y. Sun, and J. R. Cavallaro, "Parallel Nonbinary LDPC Decoding on GPU," *2012 IEEE Asilomar Conference on Signals*, Systems, *and Computers*, Pacific Grove, CA, November 2012, (May 2012, Submitted, June, 2012, Accepted).

5. B. Yin, M. Wu, G. Wang and J. R. Cavallaro "Low Complexity Opportunistic Decoder for Network Coding,"*2012 IEEE Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, CA, November 2012, (May 2012, Submitted, June 2012, Accepted).

6. G. Wang, M. Wu, Y. Sun, J. R. Cavallaro, "GPU Accelerated Scalable Parallel Decoding of LDPC Codes," *2011 IEEE Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, CA, pp. 2053-2057, (November 2011), (Submitted, May 2011, Accepted, July 2011, Published, March 2012).

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11. C. Dick, K. Amiri, J. R. Cavallaro, R. Rao, "Design and Architecture of Spatial Multiplexing MIMO Decoders for FPGAs", Invited Paper, *2008 IEEE Asilomar Conference on Signals, Systems, and Computers*, pp. 160-164, Pacific Grove, CA, (October 2008).

12. M. Myllylä, M. Juntti, J. R. Cavallaro, "Implementation and Complexity Analysis of List Sphere Detector for MIMO-OFDM Systems," *2008 IEEE Asilomar Conference on Signals, Systems, and Computers*, pp. 1852-1856, Pacific Grove, CA, (October 2008).

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2. M. Brogioli, M. Gadhiok, J. R. Cavallaro, "Design and Analysis of Heterogeneous DSP/FPGA Based Architectures for 3GPP Wireless Systems," IEEE Real-Time and Embedded Technology and Applications Symposium; Work-in-Progress Sessions, pp. 29-32, San Jose, CA, (April 2006).

3. J. R. Cavallaro, M. C. Brogioli, A. de Baynast, P. Radosavljevic, "Reconfigurable Architectures for Wireless Systems: Design Exploration and Integration Challenge," Wireless World Research Forum (WWRF-12), Toronto, Canada (November 2004).

4. J. R. Cavallaro, P. Radosavljevic, "ASIP Architecture for Future Wireless Systems: Flexibility and Customization," Wireless World Research Forum (WWRF-11), Oslo, Norway (June 2004).

5. M. L. Leuschen, J. R. Cavallaro, I. D. Walker, "Testing on the Curve: Nonlinear Analytical Redundancy for Fault Detection," *Proc. Ninth ANS Topical Meeting on Robotics and Remote Systems*, Session 22, Paper F131, Seattle, WA (March 2001).

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