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Abstract—In this article, a new soft switching isolated push–pull dc–dc converter using a three-winding transformer is proposed. The proposed hybrid resonant and pulse width modulated converter employs a conventional push–pull structure in the primary side, a voltage doubler in the secondary side, and a bidirectional switch besides the transformer, altogether helping offer a high efficiency over a wide range of input and output voltage signals with an unsophisticated fixed-frequency control mechanism. The primary-side switches are commutated under zero voltage switching with low switching current and the secondary-side diodes are commutated under zero current switching. In this article, we present an in-depth analysis of various operation modes and design constraints. Our analysis is further complemented with a comprehensive reliability evaluation of the proposed converter under various short circuit and open circuit fault scenarios. Different from the previous research, the derated operating states of the proposed converter are detailed and characterized in the reliability evaluation. Finally, the theoretical analyses are verified via tests and experiments performed on a 280 W/34.7 kHz prototype.

Index Terms—Faults, mean time to failure (MTTF), open circuit (OC), reliability analysis, short circuit (SC), soft switching isolated push–pull dc–dc converter.

I. INTRODUCTION

ISOLATED dc–dc converters have been widely utilized in renewable energy systems, electric vehicles, aircrafts, and home appliances, such as power conditioning systems [1], [2]. The growing demand for such technologies and the intensified economic constraints in the electric industry calls for advanced mechanisms enabling efficient and low-cost designs of dc–dc converters [3]. One simple-in-control and low-in-cost class of isolated dc–dc converters is the conventional pulse width modulated (PWM) flyback dc–dc converter [4]. While cost effective with a relatively low number of components, they lack a capability for direct power transfer to the load. Some other classes of flyback converters are recommended in response, such as quasi-resonant flyback converters [5], active clamp flyback converters [6], and full soft switching flyback converters [7], to enhance the operation efficiency, but at the cost of additional number of components and sophisticated control systems.

Series resonant converters operating with direct power transfer from input source to the load, soft switching of semiconductors, and reasonably good magnetic utilization are one of the most efficient isolated-type dc–dc converters. In [8] and [9], a class of series resonant converters is recommended, where the resonant tanks help ensure that the switches turn OFF under zero current switching (ZCS) conditions. While this practice offers a higher operation efficiency, they are still bulky. In the other related literature, ZCS techniques are proposed and applied using active auxiliary cells, in which sophisticated cells and control systems are employed to commutate the switches under ZCS conditions. For instance, in [10], two auxiliary active switches are utilized in the auxiliary cell. In [11], an LLC isolated resonant converter is presented, in which the input voltage regulation and a high efficient operation are achieved over a very limited range. In [12], an optimized wide-range LLC converter is introduced, in which the operation far from the resonant frequency leads to larger circulating current and, hence, poor efficiency. In [13], one modified LLC converter is presented where high efficiency is achieved over a wide range of input voltage, but reveals a poor operation under light-load scenarios.

Push–pull dc–dc converters are the other popular class of isolated converters. In order to improve the operation efficiency in this class of isolated dc–dc converters, several soft switched topologies are introduced in the literature. In [14], a zero voltage and ZVS (ZVZCS) push–pull converter is presented, in which the primary-side switches are commutated under ZVZCS conditions, whereas the secondary-side diodes are still hard switched. In [15], a current-fed ZVZCS push–pull converter is presented, which provides zero voltage switching (ZVS) and ZCS for the primary- and secondary-side semiconductors, respectively. In [16] and [17], two ZVS push–pull converters are suggested, where ZVS of the primary-side switches is achieved, while still...
prone to the switching losses in the secondary-side semiconductors. In [18]–[20], several other topologies for soft switching push–pull converters are presented, where soft switching of the main switches is provided to reduce the switching loses. Majority of these topologies are, however, bulky—with a large number of semiconductors and intensified conduction losses.

Several research efforts can be found in the literature that evaluate the converters performance under different operating conditions and from different perspectives, e.g., reliability and mean time to failure (MTTF). In [21] and [22], the reliability performance of the interleaved PWM boost converters is assessed and compared with that of single-stage conventional boost converter. In [23], an interleaved full soft switching dc–dc boost converter is presented and its reliability performance is compared with that of the single-stage soft switching and hard switching boost converters. In [24], a conventional buck–boost converter is evaluated from reliability and MTTF points of view.

In this article, a new soft switching isolated push-pull dc–dc converter is introduced characterized with a simple resonant system, where ZVS and ZCS are achieved in the primary-side switches and secondary-side diodes, respectively. We analyze the reliability performance of the proposed converter by characterizing its derated operating states under a variety of operation conditions and short circuit (SC)/open circuit (OC) fault scenarios. Reliability performance comparisons against the similar class of converter topologies are conducted. Eventually, the proposed converter is experimentally tested with extensive analysis to verify its operational and reliability performance.

II. PROPOSED CONVERTER VERSUS STATE-OF-THE-ART PUSH–PULL CONVERTERS

The proposed soft switching push–pull dc–dc converter is demonstrated in Fig. 1. It contains two switches ($S_1$ and $S_2$) of a push–pull structure in the primary side, two diodes ($D_{o1}$ and $D_{o2}$) and two capacitors ($C_{r1}$ and $C_{r2}$) in the secondary side, one bidirectional switch ($S_3$) and a three-winding transformer with turns ratio of $n$, a magnetizing inductor ($L_m$), and a leakage inductor ($L_r$). Furthermore, one filter capacitor ($C_o$) is placed in the output load terminal. Capacitors $C_{r1}$ and $C_{r2}$ establish a voltage doubler with $D_{o1}$ and $D_{o2}$ diodes in the secondary side and also a resonant tank with inductance $L_r$. The following assumptions are considered here to simplify the operation mode analysis of the proposed converter [25]–[27].

1) All components and devices are assumed ideal.
2) The input voltage $V_i$ is assumed constant.
3) The output filter capacitor $C_o$ is assumed large enough to be considered with constant output voltage $V_o$.
4) The $C_{r1}$ and $C_{r2}$ capacitors are assumed equal, expressed by $C_r$.
5) The capacitance of $C_o$ is much larger than the capacitances of $C_{r1}$ and $C_{r2}$.
6) The nonideal transformer is modeled by an ideal transformer with the inductances of $L_m$ and $L_r$.

The proposed converter operates in four different operation modes in a half switching cycle, where the other four modes of operation are repeated symmetrically in the next half. The current flow paths of these operation modes are illustrated in Fig. 2 and the steady-state key waveforms are provided in Fig. 3.

Mode 1 ($t_0 \leq t < t_1$): This operation mode starts when switches $S_2$ and $S_3$ are turned ON, resulting in the $V_i$ voltage
across each primary winding of the transformer. Prior to this mode, the current \( i_{Lr} \) flowing through the inductor \( L_r \) is zero and the voltage \( v_{C_{r1}} \) across the capacitor \( C_{r1} \) is at its minimum. Since the output voltage is twice \( v_{C_{r1}} \), the initial condition for \( v_{C_{r1}} \) can be characterized as follows:

\[
v_{C_{r1}} \big|_{t=t_0} = v_{C_{r1}} \big|_{\text{min}} = \frac{V_o}{2} - \Delta v_{C_{r}} \tag{1}
\]

where \( \Delta v_{C_{r}} \) is the voltage ripple across \( C_{r1} \) and is equal to

\[
\Delta v_{C_{r}} = \frac{P_o T}{2 V_o C_{r}} \tag{2}
\]

where \( T \) is the half switching cycle in the proposed converter and is approximately equal to \( t_3 - t_0 \) or \( t_5 - t_4 \), and \( P_o \) is the output power. As formulated in (3) and (4), \( i_{Lm} \) and \( i_{Lr} \) increase linearly with the \( nV_i \) voltage in this operation mode, which is similar to the conventional PWM boost converter, given by

\[
i_{Lm} = \frac{nV_i}{L_m} (t - t_0) + i_{Lm} \big|_{t=t_0} \tag{3}
\]

\[
i_{Lr} = \frac{nV_i}{L_r} (t - t_0) \tag{4}
\]

where the initial condition for \( i_{Lm} \) is enforced in the following equation taking into account the symmetrical observations in its waveform at \( t = t_0 \) and \( t = t_4 \):

\[
i_{Lm} \big|_{t=t_0} = \frac{-nV_i T}{2 L_m} \tag{5}
\]

**Mode 2** \((t_1 \leq t < t_2)\): At \( t = t_1 \), the switch \( S_3 \) is turned OFF, whereas switch \( S_2 \) is still ON, transferring the input power to the output load through diode \( D_{o1} \). In this mode, the inductor \( L_r \) and the parallel combination of \( C_{r1} \) and \( C_{r2} \) capacitors resonate. The initial conditions in operation mode 2 are evaluated as follows:

\[
i_{Lm} \big|_{t=t_1} = \frac{nV_i (2D - 1)T}{L_m} \tag{6}
\]

\[
i_{Lr} \big|_{t=t_1} = \frac{nV_i DT}{L_r} \tag{7}
\]

where \( DT \) is a parameter representing the ON-time duration of the \( S_3 \) bidirectional switch in the operation mode 2 and controls the output power with fixed frequency in maximum power point tracking applications. The main resonant equations in this operation mode are formulated as follows:

\[
i_{Lr} = i_{D_{o1}} = \frac{r}{Z_r} \sin \left[ \theta_1 - \omega_r (t - t_1) \right] \tag{8}
\]

\[
v_{C_{r1}} = v_{S_{3}} = nV_i + r \cos \left[ \theta_1 - \omega_r (t - t_1) \right] \tag{9}
\]

where \( \omega_r \) and \( Z_r \) are the resonant angular frequency and characteristic impedance of the resonance between \( L_r \) and the parallel combination of \( C_{r1} \) and \( C_{r2} \), respectively, and are determined as follows:

\[
\omega_r = 2 \pi f_r = \frac{1}{\sqrt{L_r (C_{r1} + C_{r2})}} \tag{10}
\]

\[
Z_r = \sqrt{\frac{L_r}{C_{r1} + C_{r2}}} \tag{11}
\]

Then, the \( r \) and \( \theta_1 \) parameters are obtained as follows:

\[
r = \frac{V_o}{2} + \Delta v_{C_{r}} - nV_i \tag{12}
\]

\[
\theta_1 = \cos^{-1} \left( \frac{r - 2 \Delta v_{C_{r}}}{r} \right) \tag{13}
\]

The preceding equations are concluded from the resonant tank trajectory of the state variables, demonstrated in Fig. 4 and fully described in Section III.

**Mode 3** \((t_2 \leq t < t_3)\): At \( t = t_2 \), the diode \( D_{o1} \) turns OFF under ZCS condition and no power is transferred from the input source to the output load. This operation mode is employed to ensure the ZCS condition for the secondary-side diodes. Since the proposed converter always operates at a fixed frequency \((f_S = 1/2T)\) at a range close to the series resonant frequency \((f_r = \omega_r/2\pi)\), the \( i_{Lm} \) current is always small and the primary-side switches commutate under a low switching current. The current flowing in the primary-side switch \( i_{S_{2}} \) at the end of this operation mode is evaluated as follows:

\[
i_{S_{2}} \big|_{t=t_3} = \frac{n^2 V_i DT}{2 L_m} \tag{14}
\]

In this mode, the \( v_{C_{r1}} \) voltage is in its maximum as follows:

\[
v_{C_{r1}} \big|_{t=t_3} = v_{C_{r1}} \big|_{t=t_3} = \frac{V_o}{2} + \Delta v_{C_{r}} \tag{15}
\]

**Mode 4** \((t_3 \leq t < t_4)\): At \( t = t_3 \), the switch \( S_2 \) is turned OFF and the \( i_{Lm} \) current is at its maximum \((I_{Lm})\). As this operation mode is very short, it can be presumed as a current source, where the current flows through the parasitic capacitors of the primary-side switches, charging \( C_2 \) and discharging \( C_1 \) capacitors linearly. Operation mode 4 can be characterized through the following equations:

\[
I_{Lm} = \frac{nV_i T}{2 L_m} \tag{16}
\]

\[
v_{s_1} = \frac{2V_i}{n} - \frac{nI_{Lm}}{2C_1} (t - t_3) \tag{17}
\]

\[
v_{s_2} = \frac{nI_{Lm}}{2C_2} (t - t_3) = \frac{n^2 V_i T}{4 L_m C_2} (t - t_3). \tag{18}
\]
With a short time interval described in (19), the operation mode 4 ends when \( v_{S1} \) reaches zero at \( t = t_4 \). This is when the \( S_1 \) switch can be turned on under ZVS condition in the second-half switching cycle

\[
t_4 - t_3 = \frac{4L_m C_2}{n^2 T^2}.
\]

At \( t = t_4 \), one half of the switching cycle ends and the second half starts with \( S_1 \) switch turned on.

A comparison study on the operation of the proposed push–pull topology and the state-of-the-art push–pull converters is presented in Table I. The comparison is provided with regard to several factors including the number of elements, the soft switching conditions, and the voltage boost capability of the converters. Comparison results demonstrate the operation superiority of the proposed converter. According to Table I, the proposed converter assembles five semiconductors, which is lower than the competitors. Furthermore, the proposed converter topology offers soft switching transitions for both primary- and secondary-side semiconductors, similar to those suggested in [15], [18], and [20]. Considering the duty cycle and transformer turns ratio requirements, the proposed topology reveals an acceptably high voltage gain among other topologies in the literature.

### III. RESONANT TANK TRAJECTORY

In order to simplify the operational mode analysis of the proposed push–pull converter, its resonant tank trajectory including state variables of \( i_{Lr} \) and \( v_{Cr1} \) is presented in Fig. 4. As the converter starts its operation in one switching cycle \( (t = t_0) \), the converter’s operating point is at \( A_1 \) with \( i_{Lr} = 0 \) and the minimum \( v_{Cr1} \). During operation mode 1, the operating point transits from \( A_1 \) to \( B_1 \) with linear increase in \( i_{Lr} \) and under a constant \( v_{Cr1} \). In operation mode 2, the operating point moves from \( B_1 \) to \( A_2 \) on a circular path characterized by the resonance between \( L_r \) and the parallel combination of \( C_{r1} \) and \( C_{r2} \). The center point of this circular path is \( O_1 \), which is located at \( (nV_i, 0) \) with the radius \( r \)—see (12). \( \theta_1 \) is the angle formed by the initial conditions in operation mode 2—see (13). The duty cycle corresponding to switch \( S_1 \) \( (D) \) is assessed using the Pythagorean theorem on \( A_1 B_1 O_1 \) triangle as follows:

\[
\left( \frac{A_1 B_1}{2} \right)^2 = \frac{r^2 - x^2}{2}
\]

\[
x = nV_i - \frac{V_o}{2} + \Delta v_{cr_1}
\]

\[
D = \frac{1}{nV_i} \left[ \frac{2L_r P_o}{P} \left( 1 - \frac{2nV_i}{V_o} \right) \right]^{1/2}.
\]

The preceding equations demonstrate that \( D \) depends on both \( n \) and \( P_o \). Since \( D \) is small under most operating conditions, direct power transfer is achieved in the proposed converter during most of the switching cycle duration. During operation modes 3 and 4, \( i_{Lr} \) and \( v_{Cr1} \) are constant. Therefore, the trajectory path stays around the operating point \( A_2 \). This continues until operation mode 4 ends, when the second half cycle starts from \( A_2 \) with a symmetrical path transmission.

### IV. RELIABILITY ANALYSIS AND PERFORMANCE EVALUATIONS

This section elaborates the reliability assessment of the proposed push–pull converter centered on the Markov process models. The reliability analytics proposed in this research trail the following procedure:

1. characterization of the converter operating states under different fault scenarios;
2. Markov chain process for both SC and OC fault scenarios;
3. components’ failure rate assessments in each operating state considering the nonideal operation characteristics;
4. quantification of the reliability and MTTF metrics under both SC and OC fault scenarios;
5. assessment of the system overall reliability performance.

The converter’s operating states under different SC and OC fault scenarios on the components are first determined. Any SC fault scenario on the proposed converter topology results in the total system failure, represented as the absorbing state. Under OC fault scenarios on some components, however, the converter continues to function in other operating states with different power flow arrangements, represented as derated states. The introduced operating states are demonstrated in Fig. 5 and their specifications are indicated in Table II. As indicated in Table II, the OC faults on \( S_1 \) or \( S_2 \) switches, \( S_3 \) switch, and \( C_{r1} \) or \( C_{r2} \) capacitors will change the converter operating state similar...
Fig. 5. Converter’s different operating states under OC fault scenarios. (a)–(g) correspond to the OC fault operating states of 2–8 in Table II.

TABLE II
SPECIFICATIONS OF DIFFERENT OPERATING STATES UNDER OC FAULT SCENARIOS

<table>
<thead>
<tr>
<th>State #</th>
<th>Condition</th>
<th>OC Fault on Components</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Full power</td>
<td></td>
<td>Healthy (Initial State)</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>$S_1$ or $S_2$</td>
<td>Soft Switching Flyback</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>$S_1$</td>
<td>Hard Switching Push-Pull</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>$C_r$ or $C_{r2}$</td>
<td>Asymmetric Soft Switching Push-Pull</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>$S_1$ or $S_2$, and $S_2$</td>
<td>Hard Switching Flyback</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>$S_1$, and $C_r$ or $C_{r2}$</td>
<td>Asymmetric Soft Switching Flyback</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>$S_1$, and $C_r$ or $C_{r2}$</td>
<td>Asymmetric Hard Switching Push-Pull</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>$C_r$, $C_{r2}$, and $S_1$</td>
<td>Asymmetric Hard Switching Flyback</td>
</tr>
<tr>
<td>9</td>
<td>No Power</td>
<td></td>
<td>Total Failure (absorbing state)</td>
</tr>
</tbody>
</table>

To that observed in flyback converters, hard switching, and asymmetric operations, respectively.

With the operating states identified, the Markov chain architecture corresponding to the proposed converter under SC and OC fault scenarios is achieved as illustrated in Fig. 6. Each transition from the operating state $i$ to $j$, which is realized due to a faulted component, is attributed a failure rate $(\lambda_{ij})$.

Operating states 2 and 9 are found as the absorbing operating states under SC and OC fault scenarios, respectively. According to Fig. 6(a), the only one failure rate $(\lambda_{12}^{SC})$ under SC fault scenarios is assessed as the summation of all failure rates of converter components under SC fault scenarios and formulated as follows:

$$\lambda_{12}^{SC} = \lambda_{S1}^{SC} + \lambda_{S2}^{SC} + \lambda_{S3}^{SC} + \lambda_{D1}^{SC} + \lambda_{D2}^{SC} + \lambda_{Cr}^{SC} + \lambda_{Trans}^{SC} + \lambda_{Co}^{SC}$$

(23)

where the parameters are corresponded to the failure rates of the switches, the output diodes, the resonant and output capacitors, and the transformer under SC fault scenarios. As one can observe from Table II and Fig. 6(b), different $\lambda_{ij}$ exist for the proposed converter as different operating states are projected under OC fault scenarios. Assuming the occurrence of SC faults, the SC-centered state-space equation is formulated as follows:

$$\frac{d}{dt} \begin{bmatrix} P_{SC}^{SC}(t) \\ P_{SC}^{SC}(t) \end{bmatrix} = \begin{bmatrix} -\lambda_{S1}^{SC} \\ -\lambda_{S2}^{SC} \end{bmatrix} \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

(24)

where $P_{1}^{SC}(t)$ and $P_{2}^{SC}(t)$ are the probabilities of operating states 1 and 2 under SC fault scenarios. Considering the fact that the converter is on a healthy operating state at the beginning of its operation, the initial value for these probabilities are equal to

$$[P_{SC}(0)] = \begin{bmatrix} 1 \\ 0 \end{bmatrix}.$$  

(25)

Since the operating state 2 is found to be the absorbing state under SC faults, the reliability of the proposed converter in such scenarios is equal to the probability of the first state as follows:

$$R_{SC}(t) = P_{1}^{SC}(t) = e^{-\lambda_{12}^{SC}t}.$$  

(26)
On the other hand, the state-space equation under OC fault scenarios on the converter components is formulated as follows:

$$\frac{d}{dt} \begin{bmatrix} P_{1}^{OC}(t) \\ P_{2}^{OC}(t) \\ \vdots \\ P_{9}^{OC}(t) \end{bmatrix} = \begin{bmatrix} -k_{1} & \lambda_{12} & \lambda_{13} & \lambda_{14} & 0 & 0 & 0 & 0 & \lambda_{19} \\ 0 & -k_{2} & 0 & 0 & \lambda_{25} & \lambda_{26} & 0 & 0 & \lambda_{29} \\ 0 & 0 & -k_{3} & 0 & \lambda_{35} & 0 & \lambda_{37} & 0 & \lambda_{39} \\ 0 & 0 & 0 & -k_{4} & 0 & \lambda_{46} & \lambda_{47} & 0 & \lambda_{49} \\ 0 & 0 & 0 & 0 & -k_{5} & 0 & 0 & \lambda_{58} & \lambda_{59} \\ 0 & 0 & 0 & 0 & 0 & -k_{6} & 0 & \lambda_{68} & \lambda_{69} \\ 0 & 0 & 0 & 0 & 0 & 0 & -k_{7} & \lambda_{78} & \lambda_{79} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -k_{8} & \lambda_{89} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \times [M]$$  

(27)

where $P_{i}^{OC}(t)$ and $P_{j}^{OC}(t)$ are the probabilities corresponding to the operating states 1–9 under OC fault scenarios, respectively, and $[M]$ is equal to

$$M = \begin{bmatrix} -k_{1} & \lambda_{12} & \lambda_{13} & \lambda_{14} & 0 & 0 & 0 & 0 & \lambda_{19} \\ 0 & -k_{2} & 0 & 0 & \lambda_{25} & \lambda_{26} & 0 & 0 & \lambda_{29} \\ 0 & 0 & -k_{3} & 0 & \lambda_{35} & 0 & \lambda_{37} & 0 & \lambda_{39} \\ 0 & 0 & 0 & -k_{4} & 0 & \lambda_{46} & \lambda_{47} & 0 & \lambda_{49} \\ 0 & 0 & 0 & 0 & -k_{5} & 0 & 0 & \lambda_{58} & \lambda_{59} \\ 0 & 0 & 0 & 0 & 0 & -k_{6} & 0 & \lambda_{68} & \lambda_{69} \\ 0 & 0 & 0 & 0 & 0 & 0 & -k_{7} & \lambda_{78} & \lambda_{79} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -k_{8} & \lambda_{89} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$  

(28)

where $k_{i}$ is equal to the summation over all failure rates in row $i$, as the sum of all elements in each row of the matrix $M$ must be zero. Similar to (25), the initial state probability under OC fault scenarios is assumed as follows:

$$[P_{OC}(0)] = \begin{bmatrix} 1 \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix}.$$  

(29)

As illustrated in Fig. 6(b), the operating state 9 is the absorbing state under OC faults. Hence, the reliability of the proposed converter under such scenarios is assessed as follows:

$$R_{OC}(t) = \sum_{i=1}^{8} P_{i}^{OC}(t).$$  

(30)

In order to evaluate the failure rates of the converter components, Table III presents different factors that influence the failure rates, including the components’ design quality ($\pi_{Q}$), environmental conditions ($\pi_{E}$), application factor ($\pi_{A}$), construction factor ($\pi_{C}$), series resistance factor ($\pi_{SR}$), and capacity factor ($\pi_{Cap}$) [25], [26]. In this article, we reasonably selected $\pi_{Q} = 8$, $\pi_{E} = 1$, $\pi_{A} = 8$, and $\pi_{C} = 1$ for the proposed converter [28], [29]. Furthermore, the electrical stress factor of a diode ($\pi_{S}$) and voltage stress factor of a capacitor ($\pi_{V}$) are enforced as follows:

$$\pi_{S} = V_{S}^{2.43}$$  

(31)

$$\pi_{V} = \left( \frac{S}{0.6} \right)^{3}$$  

(32)

where $V_{S}$ is the voltage stress ratio and is defined as the ratio of the applied reverse voltage to the rated reverse voltage across the diode. Furthermore, $S$ is the ratio of the operating voltage to the rated voltage across the capacitor.

Another important factor affecting the components’ failure rates is the temperature ($\pi_{T}$), directly driven by the power loss of the equipment ($P_{Loss}$, $P_{D}$, and $P_{Trans}$). Table IV presents the key equations to characterize the temperature factor impacts on the equipment failure rates, where $T_{j}$, $T_{C}$, $T_{HS}$, $T_{A}$, and $\Delta T$ are the junction temperature, case temperature of switches and diodes, hot spot temperature of the transformer, ambient temperature, and average temperature rise above the ambient temperature, respectively. $T_{S}$ is the switching period ($T_{S} = 2T_{s}$) and $A$ is the case radiating surface area of the transformer (in²). $R_{oJC}$ and $R_{oCA}$ (°C/W) are junction to case and ambient thermal resistances, respectively. According to [28], temperature factor of the capacitors depends on the ambient temperature, where it has a constant value of $\pi_{T} = 1.04$ under a constant ambient temperature. Table V summarizes the parameter values.

We utilized converter components in this study, which are all acquired from the available datasheets of IRFP260N, IRFP460N, and MUR1560. Eventually, numerical results presented in Table VI introduce the evaluated failure rates under SC and OC fault scenarios. The results presented in Table VI are further harnessed to evaluate the operating state probabilities under OC fault scenarios as tabulated in Table VII. Accordingly, the reliability metric of the proposed converter under SC and OC fault scenarios are assessed as follows:

$$R_{SC}(t) = e^{-151.78t}$$  

(33)

$$R_{OC}(t) = -1.42e^{-151.78t} + 2.1e^{-98.78t} - 0.56e^{-59.09t} + 1.25 \times 10^{-3}e^{-169.26t} - 0.44e^{-47.72t} + 0.01e^{-94.57t} + 1.31e^{-47.67t}.$$  

(34)

Furthermore, the MTTF index of reliability for the proposed converter under SC and OC fault scenarios is calculated as follows:

$$MTTF_{SC} = \int_{0}^{\infty} R_{SC}(t)dt = 6.6 \times 10^{3} \text{ h}$$  

(35)

$$MTTF_{OC} = \int_{0}^{\infty} R_{OC}(t)dt = 39.5 \times 10^{3} \text{ h.}$$  

(36)

Eventually, the overall system reliability and MTTF of the proposed converter topology are achieved as follows:

$$R(t) = aR_{SC}(t) + (1-a)R_{OC}(t)$$  

(37)


### Table IV

<table>
<thead>
<tr>
<th>Component</th>
<th>Circuit Model</th>
<th>Power Loss</th>
<th>Junction and Hot Spot Temperatures</th>
<th>Temperature Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switch</td>
<td>$\frac{R_{GS,sw}}{l_4}$</td>
<td>$P_{sw}^{loss} = \frac{1}{T_4} \int_{t_4}^{T_4} R_{GS,sw} i_4^2(t)dt$</td>
<td>$T_{j} = T_{c} + R_{AC} P_{sw}^{loss}$</td>
<td>$\pi_T = \exp \left[ -\frac{1925}{1.27 + 273} - \frac{1}{298} \right]$</td>
</tr>
<tr>
<td>Diode</td>
<td>$\frac{V_i}{l_2}$</td>
<td>$P_{D}^{loss} = \frac{1}{T_2} \int_{t_2}^{T_2} (V_i i_2(t) + V_j i_4(t))dt$</td>
<td>$T_{j} = T_{c} + R_{AC} P_{D}^{loss}$</td>
<td>$\pi_T = \exp \left[ -\frac{3091}{1.27 + 273} - \frac{1}{298} \right]$</td>
</tr>
<tr>
<td>Transformer</td>
<td>$\frac{R_{trans}}{l_{trans}}$</td>
<td>$P_{trans}^{loss} = \frac{1}{T_{trans}} \int_{t_{trans}}^{T_{trans}} R_{trans} i_{trans}^2(t)dt$</td>
<td>$T_{j} = T_{c} + 1.2\Delta T \frac{125 P_{trans}^{loss}}{A}$</td>
<td>$\pi_T = \exp \left[ -\frac{0.11}{8.617 \times 10^{-3}} \frac{1}{1.27 + 273} - \frac{1}{298} \right]$</td>
</tr>
</tbody>
</table>

Note: All temperature factors are in degrees centigrade.

### Table V

<table>
<thead>
<tr>
<th>Components</th>
<th>Parameters and Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1$ and $S_2$</td>
<td>$R_{GS,sw} = 0.04 \Omega$, $C_s = 603 pF$, $R_{AC} = 0.5 \sqrt{W}$, $R_{AC} = 40.5 C/W$ and $\lambda_b = 0.06$</td>
</tr>
<tr>
<td>$S_1$</td>
<td>$R_{GS,sw} = 0.27 \Omega$, $C_s = 870 pF$, $R_{AC} = 0.5 \sqrt{W}$, $R_{AC} = 40.5 C/W$ and $\lambda_b = 0.06$</td>
</tr>
<tr>
<td>$D_{d1}$ and $D_{d2}$</td>
<td>$V_j = 1.5V$, $R_D = 0.02 \Omega$, $R_{AC} = 2.0 \sqrt{W}$, $R_{AC} = 62 C/W$ and $\lambda_b = 0.0038$</td>
</tr>
<tr>
<td>$C_{s1}$, $C_{s2}$ and $C_s$</td>
<td>$\lambda_b = 0.002$</td>
</tr>
<tr>
<td>Transformer (Trans)</td>
<td>$R_{trans} = 0.038 \Omega$, $A = 0.22 m^2$ and $\lambda_b = 0.049$</td>
</tr>
</tbody>
</table>

Note: $\lambda_b$ is in failures per $10^6 h$.

### Table VI

<table>
<thead>
<tr>
<th>Calculated Failure Rates Under SC and OC Fault Scenarios</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>$\lambda_{SC}^{a}$</td>
</tr>
<tr>
<td>$\lambda_{SC}^{b}$</td>
</tr>
<tr>
<td>$\lambda_{33}$</td>
</tr>
<tr>
<td>$\lambda_{44}$</td>
</tr>
<tr>
<td>$\lambda_{99}$</td>
</tr>
<tr>
<td>$\lambda_{25}$</td>
</tr>
<tr>
<td>$\lambda_{26}$</td>
</tr>
</tbody>
</table>

Note: All failure rates are in failures per $10^6 h$.

MTTF is illustrated with respect to $a$. One can see from Fig. 7 that with the increase in $a$, the converter reliability and MTTF decrease primarily driven by the absorbing states under all SC fault scenarios.

In order to further verify the reliability performance of the proposed converter against other topologies, a comparison is made with its full-bridge topology in Fig. 8 for $a = 0.9$ and $a = 0.7$. The proposed converter reveals a higher reliability performance than that by its full-bridge topology, the reasons for which are twofold. First, the reliability performance decreases in series combination of components, where a fault on one will result in a total system failure. This combination exists in the full-bridge converter, when two switches are simultaneously turned ON in series. Second, a full-bridge topology has two additional primary-side switches with half voltage stress and the same current flowing through, and compared to the proposed push–pull converter, generates a high switch conduction power loss particularly under a higher transformer turns ratio. It can be concluded from the presented results that the switches (with high failure rates) are the most critical components in power electronic converters affecting the system reliability the most.
TABLE VII
OPERATING STATE PROBABILITIES UNDER OC FAULT SCENARIOS [30]

<table>
<thead>
<tr>
<th>Operating States</th>
<th>Probability</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{1}^{OC}$ (t)</td>
<td>$e^{-at}$</td>
</tr>
<tr>
<td>$P_{2}^{OC}$ (t)</td>
<td>$\frac{k_{2}}{k_{1}}e^{-at} - e^{-at}$</td>
</tr>
<tr>
<td>$P_{3}^{OC}$ (t)</td>
<td>$\frac{k_{3}}{k_{1}}e^{-at} - e^{-at}$</td>
</tr>
<tr>
<td>$P_{4}^{OC}$ (t)</td>
<td>$\frac{k_{4}}{k_{1}}e^{-at} - e^{-at}$</td>
</tr>
<tr>
<td>$P_{5}^{OC}$ (t)</td>
<td>$X_{1}e^{-at} + X_{2}e^{-at} + X_{3}e^{-at} + X_{4}e^{-at}$</td>
</tr>
<tr>
<td>$P_{6}^{OC}$ (t)</td>
<td>$X_{5}e^{-at} + X_{6}e^{-at} + X_{7}e^{-at} + X_{8}e^{-at}$</td>
</tr>
<tr>
<td>$P_{7}^{OC}$ (t)</td>
<td>$X_{9}e^{-at} + X_{10}e^{-at} + X_{11}e^{-at} + X_{12}e^{-at}$</td>
</tr>
<tr>
<td>$P_{8}^{OC}$ (t)</td>
<td>$(X_{13} + X_{14} + X_{15})e^{-at} + X_{16}e^{-at}$</td>
</tr>
</tbody>
</table>

Numerical Results

- $P_{5}^{OC}$ (t): $2.59e^{-0.087t} - e^{-1.79t}$
- $P_{6}^{OC}$ (t): $0.13e^{-0.318t} - e^{-1.79t}$
- $P_{4}^{OC}$ (t): $2.06e^{-0.001t} - e^{-0.23t}$
- $P_{5}^{OC}$ (t): $0.3e^{-1.79t} - 0.48e^{-0.318t} - 0.69e^{-0.318t} - 0.87e^{-0.318t}$
- $P_{6}^{OC}$ (t): $-3.32e^{-0.318t} + 0.02e^{-0.318t} + 0.02e^{-0.318t}$
- $P_{7}^{OC}$ (t): $-4.9e^{-0.318t} + 1.2e^{-0.318t} + 5.61e^{-0.318t} - 1.21e^{-0.318t}$
- $P_{8}^{OC}$ (t): $1.8e^{-0.318t} + 0.01e^{-0.318t}$

We also compared the MTTF index of reliability for the proposed converter with its full-bridge topology in Fig. 9. The presented results in Fig. 9 verify the observations in Fig. 8. One can see in Fig. 9 that the MTTF of the proposed converter and its full-bridge structure will differ significantly as $a$ decreases.

In Fig. 10, reliability of the proposed converter is compared with the reliability of other dc–dc push–pull converters under different operating conditions ($P_o = 100$ W and $a = 0.7$) and ($P_o = 250$ W and $a = 0.8$). According to Fig. 10, the following statements hold.

1) The proposed converter offers the highest reliability performance in both operating conditions.
Fig. 11. Experimental results of the proposed soft switching push–pull dc–dc converter: general observations.

Fig. 12. Experimental test of the proposed converter under different OC fault scenarios. (a) $S_1$ and $S_2$, (b) $S_1$ and $S_3$, (c) $S_3$ and $C_{r2}$, (d) $C_{r2}$ and $C_{r1}$, (e) $S_1$ and $C_{r1}$. (f) $S_1$ and $D_{o1}$.

2) Variations in $P_o$ and $a$ affect the converters reliability differently; for instance, when the output power $P_o$ decreases from 250 to 100 W, the reliability performance increases in the case of the proposed converter, whereas it is the reverse in converter topologies presented in [15] and [18].

3) The rate of reliability degradation is different among the compared converters.

V. EXPERIMENTAL RESULTS

In order to verify the performance of the proposed dc–dc converter topology under real-world operating conditions, several experimental tests are performed, the results of which are presented in Fig. 11. The test setup is characterized with $L_{m} = 7.27$ mH, $L_r = 108$ μH, $C_r = 0.33$ μF, $n = 12.5$, and the switching frequency of 34.7 kHz. In this experimental test, IRFP260N, IRFP460N, and MUR1560 are employed as the primary-side switches, secondary-side switches, and the output diodes, respectively. The experimental test results on the proposed converter are achieved with $V_i = 10$ V and $V_o = 280$ V.

Fig. 11(a) illustrates the applied gate pulses to the switches. In Fig. 11(b), the voltage across the primary-side switches are demonstrated, with the maximum value of $2V_i = 20$ V observed when in turn-off modes. These switches are commutated under the ZVS conditions in the short-interval modes of 4 and 8. In order to further verify the ZVS operation, Fig. 11(c) conjointly illustrates the voltage and the gate pulse across the $S_1$ switch. In Fig. 11(d), $i_{L_r}$ is depicted, revealing linear and sinusoidal
waveforms in modes 1 and 2, respectively. In Fig. 11(e), $v_{D01}$ and $v_{D02}$ are presented with $180^\circ$ phase shift when the ZCS turned off. In Fig. 11(f), $v_{CR1}$ and $v_{CR2}$, with the average values of $V_o/2$ and a phase shift of $180^\circ$, are demonstrated, reflecting a resonant operation in modes 2 and 6. In Fig. 11(g), the input and output voltages in the proposed push–pull converter are presented. The results in Fig. 11(g) validate the promising capability of the proposed converter in constantly generating a regulated output voltage with a reasonably high voltage gain.

Additionally, we experimentally verify the claimed performance of the proposed converter in its derated operating states and under different output power scenarios. Figs. 12 and 13 demonstrate the experimental observations when different OC and SC fault scenarios are applied on various converter elements. The operating states numbered in these figures correspond to details provided in Fig. 5 and Table II.

Fig. 14 compares the power efficiency of the proposed converter with the power efficiency of other soft switching push–pull converters, indeed with the same components characteristics. According to Fig. 14, the proposed converter offers an acceptably high efficiency in comparison with other similar converters. The maximum power efficiency of the proposed converter is 95.4%, which is achieved when $P_o = 121$ W.

VI. CONCLUSION

A new soft switching isolated push-pull dc–dc converter was proposed in this article, assembling a push–pull structure in the primary side, a capacitive voltage doubler in the secondary side, and a three-winding transformer in between. Through a simple resonant tank and a bidirectional switch, the suggested topology offered ZVS for the primary-side switches with low switching currents and ZCS for the secondary-side diodes. A comprehensive analysis of the proposed converter with ideal steady-state waveforms, under different component design characteristics and soft switching capability, were conducted and extensively compared. The reliability and MTTF evaluations of the proposed converter under both SC and OC fault scenarios were evaluated. Assessments of components failure rates in different operating states were pursued centered on the Markov process principles. Under a SC fault probability of 70%, the converter MTTF was calculated as $16.5 \times 10^3$ h. Moreover, a 280-W prototype with input voltage of 10 V, output voltage of 280 V, and switching frequency of 34.7 kHz was developed that could experimentally verify the accuracy of the discussed theoretical analysis and simulation results.

The proposed analytics in this article provided insights that can help making informative decisions in designing and implementing a more reliable power electronic converter in industrial applications. With detailed theoretical, operational, and experimental analysis, the proposed soft switching push–pull dc–dc converter offers a promising operational reliability performance in many practical settings and under a wide range of real-world scenarios, including, but not limited to, open circuit faults on various components and multiple derated operating states.

REFERENCES

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