Logic Analyzer Tutorial: Using the Agilent 16902B Logic Analysis System

Created at GWU by Thomas Farmer

Objectives:
- Learn to operate Agilent 16902B Logic Analyzer
- Attach simple CMOS chip to Logic Analyzer
- Use Logic Analyzer's Pattern Generator to provide stimulus to CMOS chip
- Use Logic Analyzer to record results of stimulus from CMOS chip
- Download CMOS Chip data from Logic Analyzer to USB device

Assumptions:
- Student has been given a demonstration of the Agilent Logic Analyzer prior to working with the system
- Note: ALL STUDENTS MUST BE TRAINED BY THE GTA PRIOR TO WORKING ON THIS TUTORIAL
- Student has access to the Agilent 16902B Logic Analyzer
- Student has checked out the Agilent 16902B Logic Analyzer Cable-set from the Tompkins equipment room

Introduction:

The ASIC design flow is as follows:

```
Specification ▼
RTL Coding and Simulation ▼
Logic Synthesis ▼
Optimization ▼
Gate Level Simulation ▼
Static Timing Analysis ▼
Place and Route ▼
Static Timing Analysis ▼
Preliminary Netlist Handoff ▼
```

In this lab, we are just after this step in the ASIC Flow

Throughout ECE 128 you have worked through the entire ASIC design flow process. After you have placed & routed a design, performed a timing analysis (tested after place & route with all layout parasitics), you would send a design out to a foundry to have it fabricated (that is the known as the Netlist Handoff). Once the chip returns, the next step is to test the chip and see if it operates as you have designed.

In ECE 126 you designed, laid out, and simulated a full-custom ASIC circuit. That circuit has been fabricated by the foundry aggregation service: MOSIS. It will be returned to GW shortly and you will begin testing and verifying that it is working as you designed. Since your design was entirely digital, you will use a testing device known as a Logic Analyzer to test your MOSIS chip.

This lab provides instruction on how to use an Agilent 16902B Logic Analyzer system with a built in pattern generator. In this lab a simple CMOS 2-input AND gate will be used as an example test circuit. You will be given two sample CMOS circuits to test and write a small report on as part of this laboratory. This will provide you with enough experience to test your own ECE 126 chip once it returns from the MOSIS service using the Agilent Logic Analyzer.
Part I: Setup Logic Analyzer Hardware

Hardware Overview:

The Agilent 16902B Logic Analyzer at GWU consists of two internal components:

- 16720A – Pattern Generator Board
- 16911A – Logic Analyzer Board

The Pattern Generator board allows the user to provide custom stimulus (test input) to his/her Device Under Test (DUT), e.g. - your ECE 126 Chip. The Logic Analyzer board allows the user to ‘analyze’ the output of the DUT due to the stimulus.

**NOTE**: You will need to go to the Tompkins Hall equipment room (TOMP 303) and check out the “Agilent logic analyzer 16902B” cable set. This will have various adapters that will adapt the output cables of the logic analyzer to connect to a CMOS chip. You will need to bring your GWU id, sign out the equipment and be responsible for its safety during your use. If anything is missing from the cable-set (you will see a manifest on the box) let the lab staff and GTA know immediately.

1. Setting up the Pattern Generator Cables/PODS:

The Logic Analyzer has two sets of cables. The first set are “output” cables (numbered 1-6), that belong to the internal pattern generator. The picture in figure 1.1 below shows the output cables that belong to the pattern generator. Notice that there are 7 output cables, the first are labeled 1-6. The seventh cable is labeled “clk”.

![Fig 1.1 – Cables coming from Internal pattern generator (from inside logic analyzer chasis)](image-url)
a) In the Logic Analyzer Cable-Set that you checked out from the Tompkins equipment room, look for the part labeled: “10477A 3.3 Volt clock Pod.” It will look much like the picture in figure 1.2.

![Fig 1.2 – Pattern Generator POD](image1)

b) Attach the CLOCK POD to the cable labeled: “CLK” coming from the logic analyzer's internal pattern generator. Fig 1.3 shows an example (but the picture used has different labels)

![Fig 1.3 – Example of attaching POD-to-LEAD adapter (left) to POD (center) to Pattern Generator cable (right)](image2)

c) Finally attach the 11 wire “rainbow” POD-to-LEAD adapter to the 10477A CLOCK POD, as shown in figure 1.3. Make sure the 'striped row' of wires faces the top of the POD (the stripped wires are GND wires), this is shown in figure 1.4.
d) Now, attach the 10483A/10466A 3-State 3.3V **DATA POD (not CLOCK POD)** to the cable labeled “1” from the internal pattern generator, as shown in figure 1.5 below.

e) Also, attach a POD-to-LEAD adapter to the **DATA POD** you just attached, ensure GND striped wires are facing upwards as in figure 1.4.
2. Setting up the Logic Analyzer Cables/PODS:

We will now hook up the cables leading from the internal logic analyzer. Attached to the logic analyzer, you should see a group of four cables, labeled: Pod 1-4 (see figure 1.6).

![Fig 1.6 – Cables coming from Internal logic analyzer (from inside logic analyzer chassis)](image)

1. In the Logic Analyzer Cable-Set that you checked out from the Tompkins equipment room, look for the cable in figure 1.7, it has 17-wires and is called a: flying leads adapter cable

![Fig 1.7 – Logic Analyzer’s Flying Lead Adapter Cable](image)

2. Attach a flying lead cable to ‘POD #1’ from figure 1.6. These cables are interchangeable, so you may attach flying lead adapter ‘POD 3 Data + L clock’ to POD 1 on the logic analyzer cable.
   - Note, just be sure to attach an adapter cable to POD #1

3. The logic analyzer is now completely setup, we need to attach it to a DUT, proceed to the next section
Part II: Attach CMOS device (DUT) to Logic Analyzer

In this tutorial, we will be using a CMOS Quad 2-input AND gate as our DUT. It has a 14-pin package, that has the PIN layout as shown in figure 2.1 below. For this tutorial, we will only be testing the first AND gate in the package. Thus the input pins are #1 & #2, and the output pin is #3.

![Fig 2.1 – CMOS AND Gate in 14-pin package](image)

This tutorial assumes you are working in Tomkins Hall room 307. A bread-board has been provided and should be in front of the logic analyzer for your use. Plug your DUT into a breadboard for testing, this is safer than working without one, so you do not accidentally short out the logic analyzer.

1. Provide POWER to the chip

A logic analyzer is not meant to provide supply voltage to your DUT. If you attempt to do so, your chip may draw more current than the logic analyzer can supply. So for any DUT, you will need to provide VCC & GND from an external power supply.

In the Tompkins labs, Agilent Power supplies are readily available. In room 307 (where this tutorial expects you to be working), a power supply is available on the shelf above the Logic Analyzer. Attach VCC=3.3VDC to your CMOS chip. Also attach GND=0V to your DUT. In the example in figure 2.1, PIN 14 is VCC, and 7 is GND.

2. Attach Pattern Generator to your DUT:

   a) Using the "POD-to-LEAD" adapter, attach output wire #0 from the Pattern Adapter's 10483A/10466A DATA POD to PIN #1 on the AND gate DUT, as illustrated in figure 2.2.

![Fig 2.2 – Pattern Generator Attached to DUT input pins](image)
b) Using the “POD-to-LEAD” adapter, attach output wire #1 from the Pattern Adapter’s 10483A/10466A DATA POD to PIN #2 on the AND gate DUT, as illustrated in figure 2.2.

c) Attach the 'striped' wire from the POD-to-LEAD adapter from the 10483A/10466A Data POD to the GND pin of your DUT, as illustrated in figure 2.2. Note, all components (the DUT, and all cables) must share a common-ground point. This is true for any testing you do with the logic analyzer.

d) In this example, our DUT does not have a CLK pin. If your DUT has a CLK, you would attach the “POD-to-LEAD” adapter, output wire: CLK from the Pattern Adapter’s 10477A CLOCK POD, to your DUT.

3. Attach Logic Analyzer to your DUT:

The pattern-generator provides stimulus to your DUT. We now need to attach the logic analyzer cables to your DUT to monitor the output of the pattern generator & the DUT’s response to the stimulus.

a) Attach wire #0 from the “Flying Lead Adapter Cable” attached to “POD #1” on the logic analyzer cable, to PIN #1 on the DUT, as illustrated in figure 2.3.

b) Attach wire #1 from the “Flying Lead Adapter Cable” attached to “POD #1” on the logic analyzer cable, to PIN #2 on the DUT, as illustrated in figure 2.3.

c) Attach wire #2 from the “Flying Lead Adapter Cable” attached to “POD #1” on the logic analyzer cable, to PIN #3 on the DUT, as illustrated in figure 2.3.

d) Attach wire: Gnd from the “Flying Lead Adapter Cable” attached to “POD #1” on the logic analyzer cable, to PIN #7 on the DUT, as illustrated in figure 2.3. (or just wire to power supply’s ground)

By attaching the analyzer to pins 1 & 2, we will be able to see what the pattern generator is producing. The analyzer attached to pin #3 will allow us to see what the DUT is producing.
Part III: Configure Logic Analyzer to Test CMOS device (DUT)

1. If Logic Analyzer is off, turn the system on by pressing the button on the front panel

2. Once Windows loads, it should automatically login and startup the logic analyzer software
   a) If it does not login automatically, login using:
      - username: ece128
      - password: ece128
   b) If the logic analyzer software does not automatically startup, from the desktop, click on the icon:
      - Agilent Logic Analyzer - GW DEFAULT

3. Once the logic analyzer software loads, you will see the following screen:

   ![Logic Analyzer Screen]

   1. The top 'module' box, labeled: “My 16720A” represents the internal **pattern generator** card
      - This will provide 'stimulus' or a 'test pattern' to your CHIP
   2. The bottom 'module' box, labeled: “My 16911A-1” represents the internal **logic analyzer** card
      - This will record output signals from your CHIP in response to the stimulus you create

CONFIGURING THE PATTERN GENERATOR MODULE:

4. Click on the 'down arrow' icon of the pattern generator module:

   ![Pattern Generator Module]

   a) From the menu, choose: Setup → Bus/Signals
   b) The pattern generator **buses/signals** setup window will open

   ![Pattern Generator Setup Window]
c) You will notice there are 6 **PODS**, 1 per 'data pod' connected the pattern generator's output wires. Each POD has 8 output ports (0-7), because each 'data pod' has 8 outputs.

d) Scroll all the way to the right until you reach “**Slot A Pod1**”
   i. Check the boxes below that you will need to test your DUT. If you have 2 input pins, you will click below #s 0 & 1 as shown in the example above. Since we'll be testing a 2-input AND gate in this tutorial, only 2 inputs are needed.
   ii. Click OK to move onto the next window

4. Again, click on the 'down arrow' icon of the pattern generator module:
   a) From the menu, choose: Setup → Clocking

   ![Pattern Generator Setup](image)

   b) Set the clock frequency to match the clock frequency of your DUT. Note, even if your device is combinational, it still has a frequency at which the data must be presented to the chip.

   c) Click OK to move onto the next window

   **d) Note: If your DUT has a CLK pin, and you've attached the “CLK” wire from the Pattern Generator's CLK POD to your DUT, this box here is where you control its frequency.**
5. Again, click on the 'down arrow' icon of the pattern generator module:

- From the menu, choose: Setup → Sequence
- This is where you will setup the test vector (or pattern) to stimulate your DUT

Under the 'My Bus 1' column, click on the title bar: 'Hex,' change it to be: BINARY

Right click on Line #4, click 'insert line after' to add another line (repeat to get 4 test rows)

You can directly type the test patterns in the rows. Or, you can have the software auto-generate a test pattern for you.

- To auto-generate, right Click on the 'My Bus 1' column, click on: 'FILL'
- Change 'type of fill' to 'count'
- Change 'starting patterns' to 'binary'
- Change 'starting line' to #3
- Change 'vectors to generate' to 4
- Change 'edit mode' to 'overwrite'
- Click FILL, then CLOSE

Your bus should now look like the following, with vectors filled in from 0 to 3 (in binary):

Click “OK” on the bottom of the “Sequence” window, all settings for the pattern generator are now complete.
6. Back on the 'Modules Overview' screen, click on the down-arrows icon on the 'My 16911A-1' logic analyzer module:

   a) From the menu, choose: Setup → Buses/Signals
   b) On the screen, you'll see 4 PODS. Each one corresponds to the 4 POD wires connected to the logic analyzer board.

   c) Each POD has 16 pins, that map to the 16 'flying leads' or wires attached to each POD
   d) In the Buses/Signals window, check only pins 0, 1, 2 (as show below)
e) Click on the 'Threshold: TTL' bar and change selection to: “LVCMOS 3.3V”

f) Press OK on the box, and OK on the buses/signals box
RUNNING THE TEST:

7. Back on the overview screen, click on the down-arrows icon on the 'My 16911A-1' and choose: New Window → Waveform

   a) Once you see the Waveform window open up, click on the ‘run/repetitive’ icon. It is the green play button icon at the top of the screen with a ‘loop’.

   b) The ‘LOGIC analyzer 16911A-1’ is now listening for output from your DUT

   c) Minimize, but do NOT close the waveform window

8. Launch the pattern generator by going back to the overview screen, click on the 'My 16720A-1', and click on the “Seq” icon

   a) Click on the “Run Rep.” green button on the bottom of the sequence window

   b) Make certain that your DUT has “VDD” and “GND” properly connected to it from an outside power supply, as discussed earlier in the tutorial
9. Return to the logic analyzer's waveform window, you will see #'s flying across the screen.
   a) Click on the red stop button at the top of the screen to stop capturing data
   b) Expand the 'bus' by clicking on the “+” sign on the left hand side of the screen, you should see the 3 pins you selected when you setup the logic analyzer's input pins

c) Click on the “go to beginning of data” button at the top of the waveform window

d) Click on the “zoom out” button at the top of the waveform window

e) Click on the “zoom out” button at the top of the waveform window, keep clicking until data begins to become visible in the waveform window as follows:

f) The waveforms above show that the AND gate is working. The top two lines represent the output from the pattern generator, and the bottom waveform shows the output from the AND gate. Inputs 00, 10, and 01 produce 0, input 11 produces a 1 (see above graph).

g) On the top of the waveform window, there are markers. You can drag the markers around the data you wish to export in the next portion of the tutorial.
EXPORTING DATA:

10. Minimize the waveform window and return to the pattern-generator

11. Open the 'sequence' setup window, and press STOP, to stop it from stimulating the chip
   a) Click OK and close the pattern generator

12. Return to the logic analyzer’s waveform window
   a) To export the data in the waveform window, you can take a screen shot (press print screen), or export the data to a CSV format that MS Excel can read.
   b) To export the data from the waveform window, choose: File->Export
      i. Choose Standard CSV format:

      ![Export dialog box]

      ii. Press OK and save this to a USB flashdrive (you can insert flashdrives into the front of the logic analyzer
      iii. Once you have the data out, you can import it into MS excel, simvision, or cadence’s spectre waveform window.
Part IV: Lab Assignment

- Before testing your MOSIS CMOS chip, from your ECE 126 course, you must test 2 simple CMOS chips
- If your GTA has not provided them to you, go to the Tompkins Equipment room on the 3rd floor. Ask for 2 stock 14-pin CMOS chips:
  1. With combinational logic only (a NAND gate, AND, NOR, etc)
  2. With sequential logic (D-Flip/Flop, counter, etc)
- Look up and print out the SPEC sheet from the manufacturer’s website
- Test the DUT using the information from the SPEC (ensure it can work at 3.3V) on the logic analyzer
  - The SPEC will tell you the PIN mapping
  - The SPEC will tell you how ‘fast’ the chip can operate, e.g. 10 MHz is typical
  - The SPEC will tell you about the setup & hold times of any sequential chip
- Hand in a report on the 2 CMOS chips with the following:
  1. Excerpt from the SPEC sheet showing: type of chip, necessary stimulus
  2. Printout of the waveforms from the logic analyzer, showing the DUT is working as SPEC’ed
  3. Summarize the data from the waveforms in a simple table, so it can easily be verified by GTA
- Note: if the GTA cannot read the printouts of these waveforms, the student loses all credit
- This work is due at the beginning of lab, printed, and stapled. No lateness or excuses will be accepted for this work.
- If you are stuck and do not understand how to do something after reading this tutorial, consult the Agilent 16902B Logic Analyzer Help files that are available on the Logic Analyzer itself before contacting your GTA.

- **This is not group work, each student must submit his/her own original report.**

Part V: References

- The Agilent 16902B Logic Analysis System Help files were used extensively to create this tutorial