Statistical Study on the Schottky Barrier Reduction of Tunneling Contacts to CVD Synthesized MoS₂

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Supporting Information

ABSTRACT: Creating high-quality, low-resistance contacts is essential for the development of electronic applications using two-dimensional (2D) layered materials. Many previously reported methods for lowering the contact resistance rely on volatile chemistry that either oxidize or degrade in ambient air. Nearly all reported efforts have been conducted on only a few devices with mechanically exfoliated flakes which is not amenable to large scale manufacturing. In this work, Schottky barrier heights of metal-MoS₂ contacts to devices fabricated from CVD synthesized MoS₂ films were reduced by inserting a thin tunneling Ta₂O₅ layer between MoS₂ and metal contacts. Schottky barrier height reductions directly correlate with exponential reductions in contact resistance. Over two hundred devices were tested and contact resistances extracted for large scale statistical analysis. As compared to metal-MoS₂ Schottky contacts without an insulator layer, the specific contact resistivity has been lowered by up to 3 orders of magnitude and current values increased by 2 orders of magnitude over large area (>4 cm²) films.

KEYWORDS: MoS₂, tunneling insulator, low-resistance contact, CVD synthesis

Two-dimensional (2D) layered materials ranging from zero bandgap graphene to wide bandgap insulators such as boron nitride offer new opportunities in the field of nanoelectronics with its rich variation of physical properties. Although graphene has been the most widely studied 2D material, its lack of a bandgap and the resulting leakage current of graphene transistors severely limits its use. 2D layered materials such as transition metal dichalcogenides (TMDs) provide a solution to this dilemma as most TMDs have a bandgap while retaining the ideal qualities of ultrathin 2D materials. Layered TMDs represent the ideal channel material for device scalability as their few-atom thick layers devoid of surface dangling bonds will be robust against short-channel effects down to very short gate lengths for ultrathin short channel devices.1,2

Although TMDs exhibit excellent intrinsic properties for device scaling, creating high-quality, low-resistance contacts is an open challenge in the development of 2D layered materials for electronics applications. While metal contacts to semimetals such as graphene have proven to be less problematic,3 metal contacts to semiconducting TMDs have proven to be more challenging due to Schottky barrier formation.4,5 Conventional substitutional doping method for decreasing the contact resistance of bulk semiconductors is not suitable for low-dimensional materials as doping impurities introduce large strain to the lattice as well as additional defect sites that lower carrier mobility.6 Previous studies show that even small Schottky barriers have significant impact on the device current drive.7 In fact, the high resistance of metal-2D semiconductor contacts have largely been attributed to sizable Schottky barriers4,5 and Fermi level pinning4,7,8 upon band alignment. While earlier reports have reported that gold contacts to MoS₂ are ohmic,9,10 the linear I–V relation is limited to the low voltage regime. Many subsequent reports confirm the existence of sizable Schottky barriers at the contacts.4,5 Experimental evidence of Fermi level pinning also has been presented for various metal-2D semiconductor contacts and the pinning is believed to be caused by gap state formation.5,7,8

Various methods have previously been used to reduce the contact resistance of transistors with TMD channels. Chemical adsorption doping techniques such as the use of NO₂ gas ambient11 or potassium ions12 to dope contact regions of WS₂-based devices have been shown to reduce contact resistance. Low work function metals have been used as contact metals to form improved contacts with thin MoS₂ flakes, resulting in higher carrier injection.4 However, air stability is a major issue with these techniques because adsorbed chemical species may desorb from the surface and the chemical species may react with oxygen and water molecules upon prolonged exposure to ambient air.13,14 Similarly, low work function metals are susceptible to oxidation.15

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A robust, air-stable technique to reduce the contact resistance is to use metal—insulator—semiconductor (MIS) contacts, which are formed by inserting a thin insulator layer between metal and semiconductor. Such a contact structure has previously been shown to reduce the effective Schottky barrier height of metal contacts to Si, Ge, and III–V material. The barrier height reduction in these contact structures has been attributed to the attenuation of metal induced gap states (MIGS) in the insulator and/or electronic dipole formation at the insulator-semiconductor interface.

In this work, a systematic study of the application of MIS contacts has been conducted on a large batch of MoS2 devices fabricated using CVD grown large area cm2 scale four-layer MoS2. True Schottky barrier heights were extracted at flat band gate bias conditions for various MIS contact insulator thicknesses. Over 200 two terminal transfer length measurement (TLM) structures were fabricated and measured to present the statistical variation of specific contact resistivity. Ta2O5, which has a low conduction band offset to MoS2, has been used as the MIS contact insulator (Supporting Information, Figure S1). Large area (>4 cm2), uniform four-layer MoS2 has been synthesized by CVD method, transferred, and patterned. (Supporting Information, Figure S2 and S3). Although large-scale syntheses of both single-layer and multilayer MoS2 are possible, multilayer (four-layer) MoS2 was used in this work because multilayer MoS2 was found to have lower contact resistance and higher on-current. This is in agreement with several reports claiming that multilayer TMDs have lower contact resistance and higher mobility due to suppression of both quantum confinement effect and interfacial Coulomb impurities scattering.

The MIS technique has also been previously applied to metal–TMD contacts by using MgO and TiO2 as the thin insulators. Although these works also showed reduction in effective Schottky barrier height, no quantitative study on the reduction of specific contact resistivity has been done. Moreover, all of these previous studies used mechanically exfoliated samples with flake sizes on the order of μm. With such small flake areas, a proper statistical study on the correlation of insulator thickness to specific contact resistivity and effective Schottky barrier height was not feasible due to the limited number of devices. Additionally, no report exists on the application of MIS contacts on larger area cm2 scale TMDs grown by synthesis techniques such as chemical vapor deposition (CVD) that are amenable to large scale manufacturing. Lastly, and most importantly, some of the early works did not take into account the influence of the gate field in their calculation of Schottky barrier height. An important goal of this work was to address the limitations of previous works, and in doing so, provide deeper insights for the application of MIS contacts.

Figure 1. (a) An optical image of the multilayer MoS2 layer synthesized on a SiO2 substrate. (b) A microscopic image of the continuous MoS2 layer with uniform contrast and its Raman spectrum (scale bar: 100 μm). The Raman peak frequency difference between the MoS2 characteristic E2g peak (407 cm−1) and the E1g peak (383 cm−1) was found to be 24 cm−1, indicative of 4–5 layer MoS2. (c) A high-resolution TEM image of the side edge profile of the MoS2 film. The film is polycrystalline as shown from the selected area electron diffraction pattern (inset). (d) Atomic force microscopy (AFM) image of MoS2 layer on SiO2 substrate. (e) MoS2 layer transferred to HfO2 substrate and patterned with lithography.

An optical image of the multilayer MoS2 synthesized on 285 nm thick SiO2 substrate is shown in Figure 1a. The film shows uniform contrast over large area in the microscope image (Figure 1b). Raman spectra taken at 10 random spots on the MoS2 film indicate that the peak frequency difference between the MoS2 characteristic E1g peak (407 cm−1) and the E2g peak (383 cm−1) was 24 cm−1, indicative of 4–5 layer MoS2 according to literature. However, it is known that Raman signature becomes less sensitive to layer thickness as the number of MoS2 layers increases, and another verification method is necessary to determine the thickness of CVD grown MoS2. The MoS2 film is characterized by atomically smooth edges and high crystallinity. From the high-resolution images at the edges (Figure 1c), we can define the thickness of the film to be four layers, a value that is in close agreement with the Raman measurement. A selective area diffraction pattern taken from ~1 μm in diameter area (Figure 1c inset) shows high-quality crystalline MoS2 with two domains rotated by about 15°, suggesting that typical domain size is about 1 μm. The thickness of the film is further confirmed by atomic force microscopy (AFM) measurement at the edge of the film (Figure 1d). These films can be transferred to an arbitrary substrate and patterned by dry etching as shown in Figure 1e.

The side view schematic of the fabricated structure is shown in Figure 2a. MoS2 films were transferred onto a 40 nm thick HfO2 substrate, and various thicknesses of Ta2O5 ranging from 0 to 5 nm, were deposited using atomic layer deposition (ALD) technique (details provided in the Supporting Information). Metal contacts (Ti/Au: 3 nm/30 nm) were then deposited and patterned to form the TLM structures (Figure 2b). The separation between contacts of the TLM structure were varied, and the resistance across the contacts were extracted from the I–V curve and plotted as a function of the contact separation. A representative plot of TLM total resistance vs contact separation is shown in Figure 2c. From such a plot, the specific contact resistivity can be extracted. Devices made from pristine, exfoliated MoS2 flakes are reported to have specific contact resistivities ρc ranging from ~3 × 10−4 Ω·cm2 to ~3 × 10−2 Ω·
From our work, we found the contact resistivity ($\rho_c$) of our CVD grown MoS$_2$ without any modification to be between $3.2 \times 10^{-3} \Omega \cdot \text{cm}^2$ and $5.9 \times 10^{-2} \Omega \cdot \text{cm}^2$ with Ti/Au contact as shown in Figure 2f. Such relatively high contact resistivity is due to the large barrier height and Fermi level pinning at the metal-MoS$_2$ contact interface as investigated in many reports. To confirm the existence of Fermi level pinning, we measured the Schottky barrier heights for another metal (Pt) contacted to MoS$_2$ and compared it with Ti contacts to extract the pinning factor (Supporting Information S4).

**Figure 2.** (a) Side view schematic of the fabricated transfer length measurement (TLM) structure. MoS$_2$ films were transferred onto a 40 nm thick HfO$_2$ substrate. Various thicknesses of Ta$_2$O$_5$, ranging from 0 to 5 nm, were deposited using ALD process. (b) Optical microscope image of the TLM structures. The device width was fixed; the separation between contacts was varied, and the resistance across the contacts was measured. (c) Typical plot of the resistance vs contact separation distance. Specific contact resistivity was extracted from the x- and y-axis intercepts. (d) Schematic band diagram of a pinned MoS$_2$ Fermi level. The metal and MoS$_2$ are in direct contact, allowing the tail of the metal electron wave function to decay into the semiconductor bandgap. (e) Schematic band diagram with Ta$_2$O$_5$ inserted between metal and MoS$_2$. The metal wave function is attenuated in the gap states. (f) Schematic band diagram with Ta$_2$O$_5$ inserted between metal and MoS$_2$. Dipole formation at the interface may also lower the effective Schottky barrier. (g) Measured specific contact resistivity ($\rho_c$) as a function of Ta$_2$O$_5$ dielectric thickness.

**Figure 3.** (a) Energy band diagrams corresponding to the applied gate biases in three distinct regions: below flat band, at the flat band, and above flat band. The contribution from the tunneling current becomes negligible only when $V_{GS}$ is at or below $V_{FB}$. (b, d) The Arrhenius plot for various gate biases when the thickness of Ta$_2$O$_5$ is 0 nm (b) and 1.5 nm (d), respectively. The slopes of these lines represent the effective Schottky barrier height, for the corresponding gate bias. (c, e) The effective Schottky barrier height as a function of gate bias when the thickness of Ta$_2$O$_5$ is 0 nm (c) and 1.5 nm (e), respectively.
0.107 which was slightly smaller than the $S = 0.113$ value extracted from the trend line shown in another article. According to the MIGS theory, the metal electron wave function decays into the semiconductor bandgap at the metal–semiconductor junction and charges the interface states of the semiconductor (Figure 2d). This pulls the intrinsic Fermi level ($E_{\text{F,int}}$) at the interface toward the charge neutrality level ($E_{\text{CNL}}$) of the gap states. A thin insulator inserted between metal and semiconductor attenuates the metal electron wave function prior to penetrating the semiconductor (Figure 2e). This results in fewer charges available to move $E_{\text{F,int}}$ toward $E_{\text{CNL}}$ as shown in Figure 2e. Another explanation for how the MIS contact structure reduces the effective Schottky barrier height is through dipole formation at the insulator–semiconductor interface. As shown in Figure 2f, interfacial dipoles of opposite polarity can effectively neutralize charges that cause the intrinsic Fermi level ($E_{\text{F,in}}$) to move toward the charge neutrality level ($E_{\text{CNL}}$), reducing the effective Schottky barrier height.

From the collective plots of total resistance vs contact separation (e.g., Figure 2c), the specific contact resistivity ($\rho_c$) for contacts with varying $\text{Ta}_2\text{O}_5$ thicknesses was extracted, and the data are shown in Figure 2g. The insertion of a 1.5 nm thick $\text{Ta}_2\text{O}_5$ layer resulted in 2–3 orders of magnitude reduction in $\rho_c$. However, as the insulator thickness is more than 1.5 nm, $\rho_c$ increased again. Such an effect is shown in Figure 2g. To understand this trend, the contact resistance of the metal/insulator/MoS2 MIS contact can be modeled as two resistances in series: the resistance due to the Schottky barrier ($R_{SB}$) and the resistance due to tunneling through the insulator ($R_T$). Without any insulator, the large Schottky barrier causes $R_{SB}$ to dominate contact resistance. By inserting a thin insulator to reduce the effective Schottky barrier height $R_{SB}$ is greatly lowered while a small $R_T$ component is added, effectively reducing the overall contact resistance. Once the insulator is increased beyond an optimal thickness, $R_T$ begins to dominate as current becomes tunneling limited, resulting in higher overall contact resistance. This is the first time such trade-offs between $R_T$ and $R_{SB}$ have been observed for metal/insulator/2D material MIS contacts, and the existence of an optimal insulator thickness for MIS contacts is confirmed.

To investigate the physical origin of lowering of $R_{SB}$, temperature-dependent carrier transport measurements were conducted, and the effective Schottky barrier heights $\Phi_{SB}$ were extracted for different insulator thicknesses. We note that the effective Schottky barrier heights $\Phi_{SB}$ of this work are not equivalent to the Schottky barrier heights of conventional metal/semiconductor junctions. Because the insulator is not accounted for in the expression for current–voltage characteristics (1) employed to determine the barrier height, the effective Schottky barrier heights extracted here are a representation of overall electrical behavior. As illustrated in Figure 3a, the band diagrams depict the contributions of thermionic emission current and thermally assisted tunneling current under various gate bias conditions. When the gate bias is above the flat band voltage, $V_{FB}$, both components contribute to the current flow during temperature-dependent measurements. The contribution from the tunneling current becomes negligible only when the gate voltage is at or below $V_{FB}$. To extract the accurate $\Phi_{SB}$ based on diode eq 1 and thermionic emission theory, $\Phi_{SB}$ must be extracted at the flat band voltage condition ($V_{GS} = V_{FB}$).

$$I_d = AT^2 \exp\left(-\frac{e\Phi_{SB}}{k_B T}\right) \left[\exp\left(-\frac{eV_{ds}}{k_B T}\right) - 1\right]$$

In this equation 1, $I_d$ is the current through the device, $A$ is the Richardson's constant, $T$ is the absolute temperature, $k_B$ is the Boltzmann constant, $q$ is the electronic charge, and $V_{ds}$ is the drain to source bias. The values of $\ln(I_d/T^2)$ at a drain bias of $V_{ds} = 1$ V for various gate biases are plotted in an Arrhenius plot (Figure 3b). The slopes of these lines directly provide the...
effective Schottky barrier height (units in eV), for the corresponding gate bias, \( V_{GS} \). This extraction is repeated for all measured gate voltages, and the slopes (i.e., effective \( \Phi_{SB} \)) as a function of the gate voltage is plotted in Figure 3c. For \( V_{GS} \) less than or equal to \( V_{FB} \) the effective \( \Phi_{SB} \) extracted from Figure 3b linearly responds to \( V_{GS} \) as shown in Figure 3c. However, as \( V_{GS} \) increases above \( V_{FB} \), the tunneling current component becomes relevant, and the plot deviates from its linear relation. Hence the accurate \( \Phi_{SB} \) extracted at flat band voltage conditions for devices without any \( Ta_2O_5 \) layer was found to be 95 meV (Figure 3c). Compared to this 95 meV barrier height, the \( \Phi_{SB} \) of devices with the lowest contact resistance was extracted to be 29 meV for a 1.5 nm thick \( Ta_2O_5 \) insulator layer as shown in Figure 3d,e.

Such analysis was repeated for other fabricated devices with various thicknesses of \( Ta_2O_5 \) (Figure 4a–c). \( \Phi_{SB} \) as a function of \( Ta_2O_5 \) insulator thickness is plotted in Figure 4d. Such change in \( \Phi_{SB} \) had a dramatic effect on the current flow across the devices because of the significant reduction in the specific contact resistivity. In Figure 4e, the current level increased by 2 orders of magnitude after the optimized thickness (1.5 nm) of \( Ta_2O_5 \) was inserted between the metal-MoS\(_2\) contact. A linear plot of the transfer curve for devices both with and without the \( Ta_2O_5 \) insulator layer is also shown in Supporting Figure S5. To gain more insight into the effect of the \( Ta_2O_5 \) layer, we extracted the threshold voltages for transistors both with and without a 1.5 nm \( Ta_2O_5 \) layer (Supporting Figure S6). From the gate response of the MoS\(_2\) bottom gate transistor, we found a slight decrease in the threshold voltage, \( V_{Th} \), before and after \( Ta_2O_5 \) layer insertion. However, the drive current increased dramatically by several orders of magnitude after \( Ta_2O_5 \) layer insertion.

In this work, we demonstrate how a low temperature (200 °C) ALD process can be used to reduce contact resistance of devices fabricated from CVD synthesized large area 2D materials. With ever-growing interest in layered two-dimensional (2D) materials, controlling material interfaces has been a critical challenge in utilizing 2D materials for their unique properties. This has been especially important for recently emerging TMDs because, unlike graphene, these materials have finite bandgaps. The tunneling insulator thickness of this MIS contact technique is highly controllable using conventional ALD tools and does not rely on low-work function metal or volatile chemistry techniques that are unstable in ambient air. This large area contact resistance study on CVD grown films will enable more facile integration of 2D material technology with today’s semiconductor technology.

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